First Demonstration of Atomic-Layer-Deposited BEOL-Compatible In_2O_3 3D Fin Transistors and Integrated Circuits: High Mobility of 113 $cm^2/V \cdot s$, Maximum Drain Current of 2.5 mA/μm and Maximum Voltage Gain of 38 V/V in In_2O_3 Inverter

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Abstract

In this work, we report the first demonstration of In_2O_3 3D transistors coated on fin-structures and integrated circuits by a back-end-of-line (BEOL) compatible atomic layer deposition (ALD) process. High performance planar In_2O_3 transistors with high mobility of 113 $cm^2/V \cdot s$ and record high maximum drain current of 2.5 mA/μm are achieved by channel thickness engineering and post-deposition annealing. High-performance ALD In_2O_3 based zero-V_{GS}-load inverter is demonstrated with maximum voltage gain of 38 V/V and minimum supply voltage (V_{DD}) down to 0.5 V. ALD In_2O_3 3D Fin transistors are also demonstrated, benefiting from the conformal deposition capability of ALD. These results suggest ALD oxide semiconductors and devices have unique advantages and are promising toward BEOL-compatible monolithic 3D integration for 3D integrated circuits.

Introduction

Indium oxide (In_2O_3) or doped-In_2O_3 are being investigated as promising channel materials for back-end-of-line (BEOL) compatible transistors for monolithic 3D integration [1], by both sputtering [2-8] and atomic layer deposition (ALD) [9-12], due to their high mobility, wide bandgap, low variability and high stability. ALD based oxide semiconductors are of special interest due to the atomically smooth surface, ultrathin thickness and the capability of conformal deposition on 3D structures. Recently, high-performance ALD In_2O_3 transistors have been demonstrated with high drain current over 2 mA/μm in both depletion-mode (D-mode) and enhancement-mode (E-mode) operations. The devices have ultra-scaled channel thickness down to 0.7 nm, high mobility of 91 $cm^2/V \cdot s$, low thermal budget below 400 ºC and stability in H_2 environment, which are highly compatible with BEOL process [10].

In this work, the performance of ALD In_2O_3 transistors are further enhanced by channel thickness (T_{ch}) engineering and post-deposition annealing. An optimized T_{ch} is determined to be 2.2-2.5 nm, achieving high mobility of 113 $cm^2/V \cdot s$ and record high maximum drain current of 2.5 mA/μm at channel length (L_{ch}) of 40 nm and V_{DS}=0.7V. A new type of 3D Fin transistors and integrated circuits based on ALD In_2O_3 are demonstrated for the first time. High-performance ALD In_2O_3 based zero-V_{GS}-load inverter presents maximum voltage gain of 38 V/V and minimum supply voltage (V_{DD}) down to 0.5 V. ALD In_2O_3 3D Fin transistors coated on SiO_2 fin-structures are also demonstrated, taking advantage of conformal deposition of ALD on 3D structures.

Experiments

Fig. 1 presents the schematic diagram of a planar back-gate In_2O_3 transistor, using the same structure as previously reported in [9, 10], which is used for circuit demonstration. The gate stack consists of 40 nm Ni as gate metal, 5 nm HfO_2 as gate dielectric, 0.5-3.5 nm In_2O_3 as semiconducting channels and 80 nm Ni as source/drain electrodes. The device fabrication process is similar to [9, 10]. The fabricated devices were annealed in O_2, N_2 or forming gas (FG, 96% N_2/4% H_2) for 30 s at different temperatures from 250 ºC to 350 ºC according to the optimized annealing conditions achieved in [10]. Fig. 2(a) shows the photo image of a fabricated In_2O_3 zero-V_{GS}-load inverter in a 5-stage ring oscillator. The circuit diagram of the In_2O_3 zero-V_{GS}-load inverter is shown in Fig. 2(b). D-mode and E-mode transistors could be achieved by threshold voltage (V_T) engineering such as plasma treatment described in [12]. E-mode device has a channel length (L_{ch}) of 2 μm while L_{ch} of D-mode devices (L_D) varies from 0.1 μm to 0.3 μm to engineer the load resistance. 3D Fin transistors with top-gate structures were fabricated on a SiO_2/Si substrate with SiO_2 fin-structures. Top-gate dielectric of 7 nm HfO_2 was formed by low-temperature ALD at 120 ºC, which is critical to form top-gate devices.

Results and Discussion

Fig. 3 shows the I_D-V_{GS} characteristics of a planar In_2O_3 transistor with L_{ch} of 1 μm and T_{ch} of 2.2 nm with O_2 annealing at 350 ºC. Fig. 4 shows the corresponding I_D-V_{DS} characteristics of the same device, exhibiting high maximum I_D of 850 μA/μm even with L_{ch} of 1 μm and well-behaved drain current saturation at high V_{DS}. Such high I_D is the result of high field-effect mobility (μ_{FE}) of 113 $cm^2/V \cdot s$, as shown in Fig. 5, extracted from the maximum transconductance (g_m) at V_{DS} of 0.05 V. Effective mobility (μ_{eff}) versus V_{GS} extracted from drain conductance (g_d) are presented in Fig. 6, which is consistent with μ_{FE}.

The mobility of In_2O_3 in this work is significantly improved compared to other ALD based oxide semiconductors [9-16]. Such high mobility is achieved by T_{ch} engineering and post-deposition annealing, as shown in Fig. 7. Average μ_{FE} > 100 $cm^2/V \cdot s$ is achieved with T_{ch} of 2.2-2.5 nm at optimized annealing conditions. μ_{FE} decreases rapidly with T_{ch} below 1 nm, mostly likely due to the enhanced surface scattering and quantum confinement effect on band structure [11]. μ_{FE} decreases at T_{ch} above 3 nm due to the higher carrier concentration and weaker gate electrostatic control, as also shown in V_T versus T_{ch} in Fig. 8. Post-deposition annealing for the reduction of oxygen vacancies in as-deposited films is needed to tune the V_T of devices with T_{ch} above 2 nm to obtain sufficiently high on/off ratio. Fig. 9 shows T_{ch}-dependent SS extracted from as-deposited devices and devices with optimized annealing conditions, exhibiting SS close to the thermal limit of 60 mV/dec at room temperature at T_{ch}~1 nm. Fig. 10 and Fig. 11 present the I_D-V_{GS} and I_D-V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 2.2 nm, exhibiting record high maximum I_D of 2.5 mA/μm under V_{DS}=0.7V and V_{GS}-V_T=4 V with optimized T_{ch} and annealing conditions.

Fig. 12 presents V_{out} versus V_{in} curve of an In_2O_3 zero-V_{GS}-load inverter with L_D of 0.3 μm at different V_{DD} from 2 V down to 0.5 V, showing well-behaved voltage transfer characteristics. The voltage gains are given in Fig. 13, achieving maximum voltage gain of 38 V/V at V_{DD} of 2 V. The midpoint voltage of the In_2O_3 zero-V_{GS}-load inverter can be engineered by tuning the load resistance and varying the channel length of the D-mode transistor, as illustrated in Fig. 14, providing the essential approach for V_{DD} and midpoint voltage engineering accordingly. Therefore, sufficiently large noise margin (NM) can be achieved, as shown in Fig. 15.

Fig. 16 shows the SEM image of an In_2O_3 3D Fin transistor with top-gate structure, capturing the gate metal, source/drain contacts and the fin-structures. Fig. 17 presents the TEM image and EDX mapping under HAADF STEM of an In_2O_3 3D Fin transistor. ALD In_2O_3 channel with T_{ch} of 1.5 nm is conformally coated on top of SiO_2 fin-structures with fin height of 180 nm and fin pitch of 130 nm. Fig. 18 shows I_D-V_{GS} characteristics of an In_2O_3 3D Fin transistor with L_{ch} of 2 μm and T_{ch} of 1.5 nm, exhibiting well-behave transfer characteristics. Fig. 19 shows the corresponding I_D-V_{DS} characteristics with maximum I_D of 180 μA/μm, normalized by device width, which is about 2 times larger than that from its top-gate planar counterpart. The 3D fin-structure provides an effective approach to increase the drive current without increasing the device area. The ultra-thin channel thickness and top-gate non-self-align structure with a large link resistance make I_D smaller than those from back-gate planar devices.

Conclusion

In summary, high-performance 3D Fin transistors and integrated circuits based on BEOL compatible oxide semiconductor by ALD are demonstrated for the first time. High mobility of 113 $cm^2/V \cdot s$ and record high maximum drain current of 2.5 mA/μm are achieved. The demonstration of 3D devices and integrated circuits suggest ALD oxide semiconductors and devices have their unique advantages over sputtering films and are promising toward BEOL-compatible monolithic 3D integration for 3D integrated circuits.

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Reference: [1] S. Datta et al., IEEE Micro, p. 8, 2019. [2] T. Kamiya et al., Sci. Technol. Adv. Mater., p. 044305, 2010. [3] S. Li et al., Nat, Mater., p. 1091, 2019. [4] W. Chakraborty et al., VLSI, p. TH2.1, 2020. [5] H. Fujiwara et al., VLSI, p. TH2.2, 2020. [6] J. Wu et al., VLSI, p. THL.4, 2020. [7] S. Samanta et al., VLSI, p. TH2.3, 2020. [8] M. Si et al., ACS Nano, p. 11542, 2020. [9] M. Si et al., IEEE EDL, p. 184, 2021. [10] M. Si et al., IEEE TED, 2021, doi: 10.1109/TED.2021.3053229. [11] M. Si et al., Nano Lett., p. 500, 2021. [12] A. Charnas et al., APL, 2021 (in press). [13] H.-I. Yeom et al., J. Mater. Chem. C, p. 6873, 2016. [14] H. Y. Kim et al., ACS AMI, p. 26924, 2016. [15] J. Lee et al., APL, p. 112102, 2018. [16] Q. Ma et al., Nanoscale Res. Lett., p. 4, 2018.

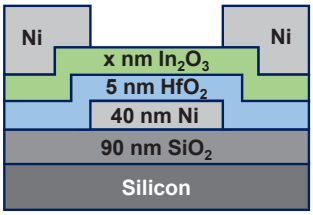

Fig. 1. Schematic diagram of a planar In_2O_3 transistor with 5 nm HfO_2 as gate dielectric and T_{ch} from 0.5 nm to 3.5 nm.

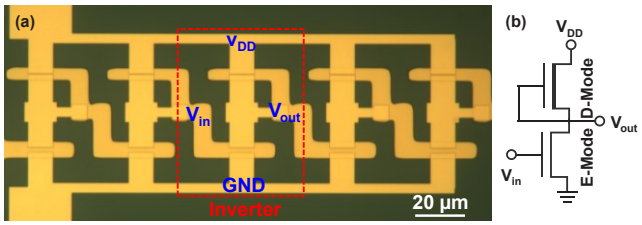

Fig. 2. (a) Photo image of an In_2O_3 zero-V_{GS}-load inverter in a 5-stage ring oscillator. (b) Circuit diagram of the In_2O_3 zero-V_{GS}-load inverter.

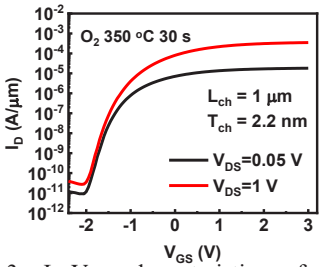

Fig. 3. I_D-V_{GS} characteristics of a planar In_2O_3 transistor with L_{ch} of 1 μm and T_{ch} of 2.2 nm with O_2 annealing.

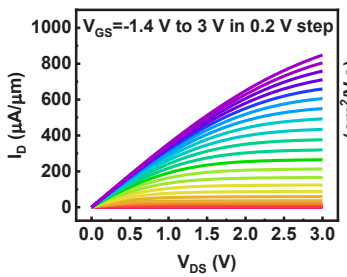

Fig. 4. I_D-V_{DS} characteristics of a planar In_2O_3 transistor with L_{ch} of 1 μm and T_{ch} of 2.2 nm with O_2 annealing.

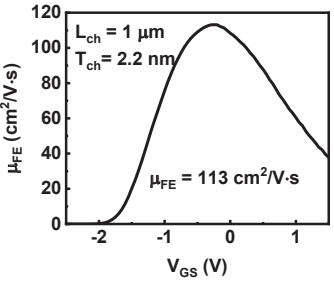

Fig. 5. μ_{FE} versus V_{GS} extracted from the maximum g_m at V_{DS} of 0.05 V from transfer curve.

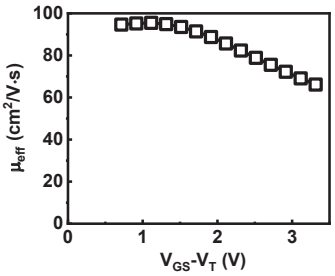

Fig. 6. μ_{eff} versus V_{GS} extracted from the g_d from output curve. The consistency of μ_{FE} and μ_{eff} is further confirmed by μ_{Hall}.[8]

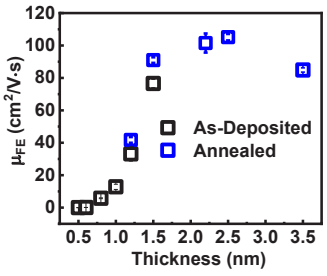

Fig. 7. μ_{FE} versus T_{ch} extracted from as-deposited devices and devices with optimized annealing conditions.

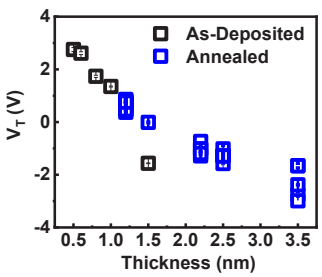

Fig. 8. V_T versus T_{ch} extracted from as-deposited devices and devices with different annealing conditions.

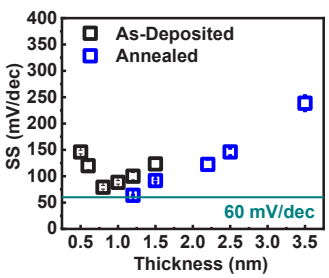

Fig. 9. SS versus T_{ch} extracted from as-deposited devices and devices with optimized annealing conditions.

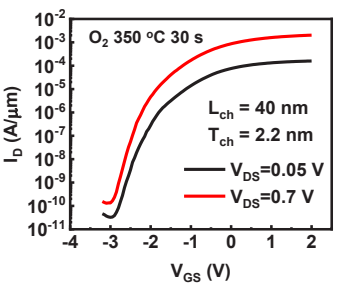

Fig. 10. I_D-V_{GS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 2.2 nm with O_2 annealing at 350 °C.

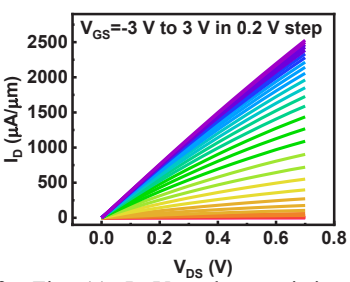

Fig. 11. I_D-V_{DS} characteristics of an In_2O_3 transistor with L_{ch} of 40 nm and T_{ch} of 2.2 nm with O_2 annealing at 350 °C.

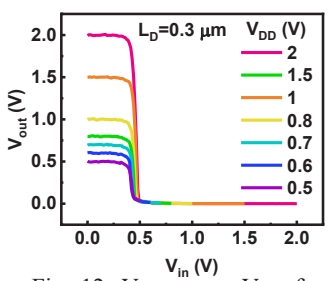

Fig. 12. V_{out} versus V_{in} of an In_2O_3 zero-V_{GS}-load inverter with L_D of 0.3 μm at different V_{DD}.

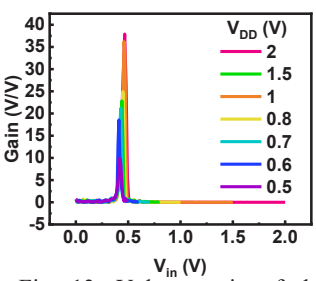

Fig. 13. Voltage gain of the In_2O_3 zero-V_{GS}-load inverter in Fig. 12 at different V_{DD}.

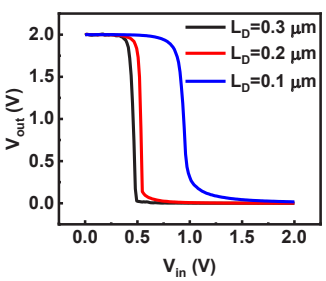

Fig. 14. V_{out} versus V_{in} of In_2O_3 zero-V_{GS}-load inverters with different L_D at V_{DD} of 2 V.

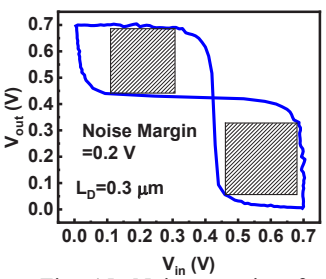

Fig. 15. Noise margin of the In_2O_3 zero-V_{GS}-load inverter as in Fig. 12 at V_{DD} of 0.7 V.

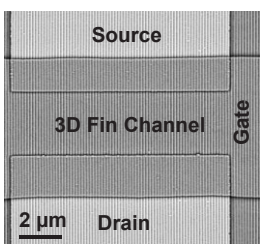

Fig. 16. SEM image of an In_2O_3 3D Fin transistor with top-gate structure. SiO_2 fin structures were fabricated by SEMATECH.

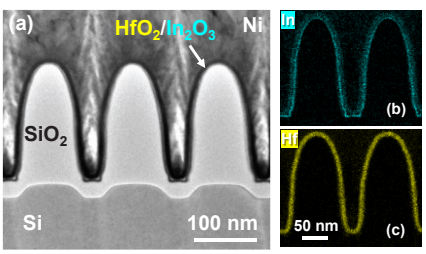

Fig. 17. (a) TEM image of a new type of 3D Fin transistor with top-gate structure and In_2O_3 channel. EDX mapping under HAADF STEM of (b) In and (c) Hf, showing the conformal coating around the Fin structure by ALD.

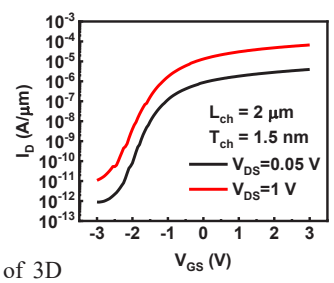

Fig. 18. I_D-V_{GS} characteristics of an In_2O_3 3D Fin transistor with L_{ch} of 2 μm and T_{ch} of 1.5 nm.

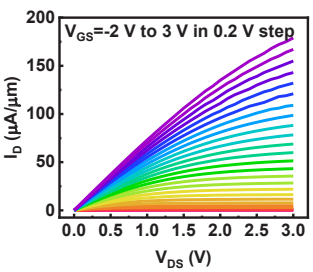

Fig. 19. I_D-V_{DS} characteristics of an In_2O_3 3D Fin transistor with L_{ch} of 2 μm and T_{ch} of 1.5 nm.