Total Ionizing Dose (TID) Effects in Extremely Scaled Ultra-Thin Channel Nanowire (NW) Gate-All-Around (GAA) InGaAs MOSFETs

Shufeng Ren, *Student Member, IEEE*, Mengwei Si, *Student Member, IEEE*, Kai Ni, *Student Member, IEEE*, Xin Wan, *Student Member, IEEE*, Jin Chen, *Student Member, IEEE*, Sungjae Chang, *Member, IEEE*, Xiao Sun, *Member, IEEE*, En Xia Zhang, *Senior Member, IEEE*, Robert A. Reed, *Fellow, IEEE*, Daniel M. Fleetwood, *Fellow, IEEE*, Peide Ye, *Fellow, IEEE*, Sharon Cui, *Senior Member, IEEE*, and T. P. Ma, *Fellow, IEEE*

***Abstract*—InGaAs nanowire (NW) gate-all-around (GAA) MOSFETs exhibit superior radiation hardness compared to planar devices and FinFETs, benefitting from reduced gate-oxide electric fields. Applied gate bias during irradiation, channel thickness, and presence or absence of a forming gas anneal can strongly affect NW device radiation hardness. Low-frequency noise measurements are carried out to probe near-interfacial oxide-trap (border-trap) densities, and TCAD simulations are performed to assist in understanding the charge trapping in NW channel devices with high-k gate dielectrics. Optimized device structures exhibit high radiation tolerance.**

***Index Terms*— $1/f$ noise, border traps, gate-all-around, high-k dielectric, InGaAs, nanowire, oxide traps, TCAD simulation.**

I. Introduction

As THE CMOS technology community is exploring solutions for 7 nm and beyond, alternative channel materials with high carrier mobility and gate structures such as nanowire (NW) gate-all-around (GAA) are promising drivers for continued scaling. III-V compound semiconductors have recently drawn wide interest for their potential application as channel materials for CMOS transistors [1], [2]. Among the various III-V materials explored, Indium Gallium Arsenide (InGaAs) is considered one of the most promising materials for N-channel MOSFETs, due to its high electron mobility, high electron velocity, and favorable band alignment. The nanowire gate-all-around (GAA) structure is a promising successor to the FinFET structure because it can provide ultimate gate electrostatic control to suppress short channel effects. InGaAs NW GAA MOSFETs integrate an InGaAs channel and high-k dielectric into the gate-all-around device structure [3]. The radiation hardness of these devices is therefore of interest for potential future space applications. Moreover, as CMOS technology is approaching the sub-10 nm node, with the possible adoption of EUV lithography, device fabrication processes can also cause radiation damage. Therefore, it is useful to understand radiation effects in future-generation device candidate technologies, such as InGaAs nanowire (NW) gate-all-around (GAA) MOSFETs.

This work provides an overview of total ionizing dose radiation effects in InGaAs nanowire (NW) gate-all-around (GAA) MOSFETs built in two different process split lots with process conditions chosen to evaluate the effects of (a) NW thickness and (b) forming gas annealing on the radiation response. We find that NW GAA devices exhibit less ionizing radiation sensitivity compared to planar and FinFET devices. Moreover, the NW channel thickness, forming gas annealing during processing, and gate biases applied during radiation all can strongly affect the radiation hardness of InGaAs NW MOSFETs. Device structures that include a forming gas anneal show excellent radiation tolerance.

II. Devices and Experiments

Both the InGaAs NW-GAA MOSFETs and the control InGaAs planar devices have ALD Al_2O_3 as the gate dielectric. Illustrative cross sections for the devices under study are shown in Fig. 1. The NW GAA MOSFETs are fabricated on an InP substrate with sequential MBE growth of the following layers: 100 nm undoped $In_{0.52}Al_{0.48}As$ etch stop, 80 nm undoped InP, 10 nm undoped $In_{0.65}Ga_{0.35}As$ channel, and 2 nm undoped InP [4]. After S/D implantation, nanowire fins are fabricated by BCl_3/Ar reactive ion etching, followed by an HCL-based release process to obtain free-standing InGaAs nanowires [4]. A 5 nm Al_2O_3 layer and a tungsten nitride (WN) gate are then subsequently deposited by ALD, followed by 400°C rapid thermal anneal in forming gas. S/D contacts are formed after the gate-etch process using electron beam lithography. The NW devices

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S. Ren, X. Sun, S.-J. Chang, S. Cui and T. P. Ma are with the Electrical Engineering Department and the Center for Research on Interface Structures and Phenomena (CRISP), Yale University, New Haven, CT 06511 USA (e-mail: shufeng.ren@yale.edu; xiao.sun@yale.edu; sungjae.chang@yale.edu; sharon.cui@yale.edu; t.ma@yale.edu).

M. Si and P. D. Ye are with Purdue University, West Lafayette, IN 47907, USA (e-mail: m.si@purdue.edu; yep@purdue.edu).

X. Wan is with Tsinghua University, Beijing 100084 China (e-mail: wan-x08@mails.tsinghua.edu.cn).

K. Ni, J. Chen, E. X. Zhang, R. A. Reed, and D. M. Fleetwood are with the Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashville, TN 37235 USA (e-mail: kai.ni@vanderbilt.edu; jin.chen@vanderbilt.edu; enxia.zhang@vanderbilt.edu; robert.reed@vanderbilt.edu; dan.fleetwood@vanderbilt.edu).

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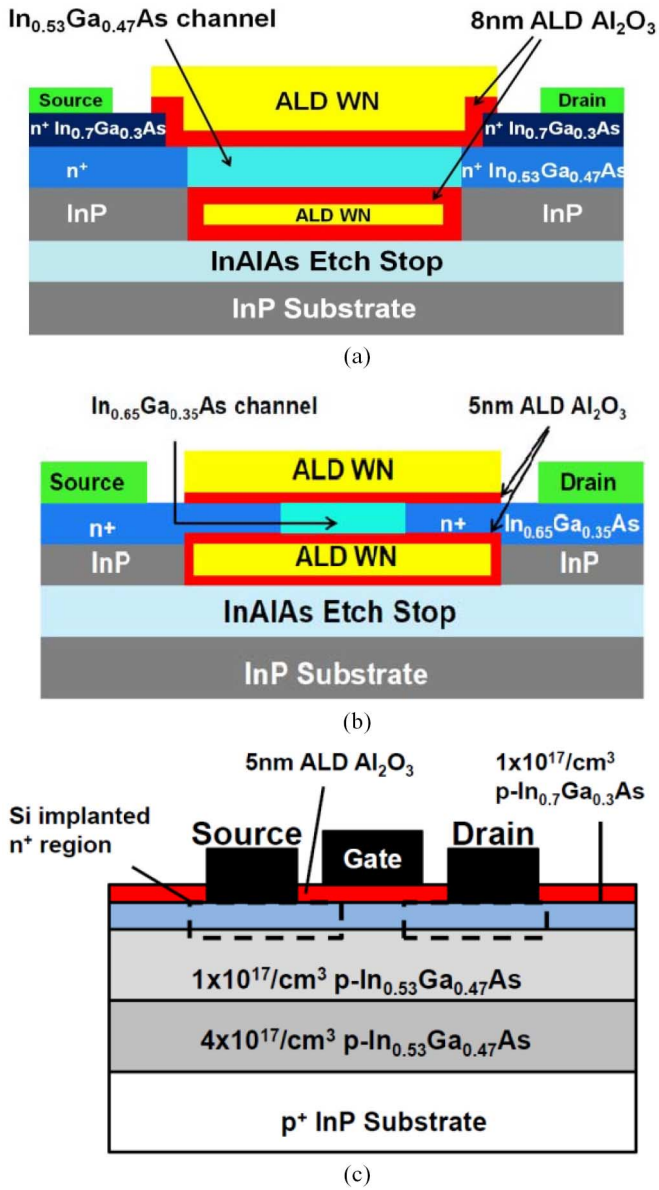

Fig. 1. Illustrative cross sections for InGaAs NW MOSFETs: (a) set A with raised source/drain structure; (b) set B with 5 nm ultrathin channel, and (c) planar InGaAs MOSFETs evaluated for comparison with the GAA structures.

in this study have channel length of 60 nm, width of 35 nm and thickness of 6 nm. The channel length of the planar devices evaluated for comparison is 110 nm.

The Set A devices, shown in Fig. 1(a), are used to study the NW thickness dependence, while the Set B devices in Fig. 1(b) are used to study the effects of forming gas annealing on the radiation hardness. Set A devices include two NW thicknesses: 10 nm and 20 nm, with otherwise identical device structure [5]. Devices in Set B are structurally identical, except that selected devices received post-metal forming gas anneal (FGA) at 400°C for 30 min. Control samples of the Set B devices did not receive FGA [6]. InGaAs planar MOSFETs and FinFETs are used as benchmark against which to compare the radiation hardness of nanowire devices because they share the same gate oxide deposition process [7].

Devices were irradiated with 10 keV X-rays at a dose rate of 31.5 krad(SiO_2)/ min using an ARACOR Model 4100 Irradiator. The irradiation was performed at room temperature with all device terminals grounded except the gate. $I_d - V_g$ transfer characteristics are monitored after each increment of dose. Radiation-induced threshold voltage shifts (ΔV_{th}) were used as a measure of the device radiation hardness. V_{th} was extracted via linear extrapolation of the $I_d - V$ curve at low drain bias (50 mV). To study gate bias effects, different gate bias conditions are applied during x-ray irradiation on InGaAs NW Set B devices with 5 nm channel thickness. The three gate bias conditions are: (1) grounded, (2) 0.5 V above V_{th}, and (3) 0.5 V below V_{th}. The source and drain were grounded for all irradiations. The three gate bias conditions correspond to three possible device operation conditions in the real circuit: on, off, all terminals grounded. In this way, we can better emulate NW device radiation responses in integrated circuit applications. Low-frequency $(1/f)$ noise measurements were used to examine the possible correlation between the radiation hardness and the oxide trap density [8]. We also carried out 3D Sentaurus TCAD simulations to obtain electrostatic information both inside the NW channel and in the gate oxide.

III. Results and Discussion

A. Comparison between NW GAA MOSFETs, FinFETs, and Planar Devices

Fig. 2 shows $I_d - V_g$ characteristics with $V_d = 50$ mV for (a) planar and (b) NW GAA devices for doses up to 1 Mrad(SiO_2). Fig. 3 compares the resulting radiation-induced V_{th} shifts (ΔV_{th}) between these two types of devices. NW devices show lower V_{th} than planar devices. This occurs because these devices did not receive a V_{th} adjust implant or incorporate gate stack that included a finely tuned metal work function. Neither of these factors are likely to affect the radiation response significantly. The NW GAA devices exhibit much smaller threshold voltage shifts ($\Delta V_{th} \sim 15$ mV), as compared with the planar devices (~ 350 mV), because of the reduced electric field in the channel and gate oxide in NW devices, as discussed below.

Fig. 4 compares threshold voltage shifts after x-ray irradiation of InGaAs FinFETs and NW GAA MOSFETs. Both FinFET and NW devices shown in Fig. 4 have the same channel thickness (10 nm) and Al_2O_3 gate dielectric thickness (8 nm). NW GAA devices exhibit smaller ΔV_{th} shifts (~ 59 mV) than that of FinFETs (~ 86 mV). The measured peak G_m, shown in Fig. 5, and the lack of significant changes in the sub-threshold swing (SS) of all types of devices during (Fig. 2) and after irradiation, suggest that 1 Mrad(SiO_2) radiation does not cause significant degradation in mobility or lead to significant interface-trap buildup in planar, FinFET or NW GAA MOSFETs.

B. Geometrical Effect: Nanowire Channel Thickness

Fig. 6 shows ΔV_{th} as a function of X-ray dose for devices with 10 nm and 20 nm NW channels, respectively. Negative ΔV_{th} is again consistent with predominantly hole trapping in the gate oxide. Also shown in Fig. 6 is the post-irradiation ΔV_{th} recovery during the subsequent room air storage. Thinner

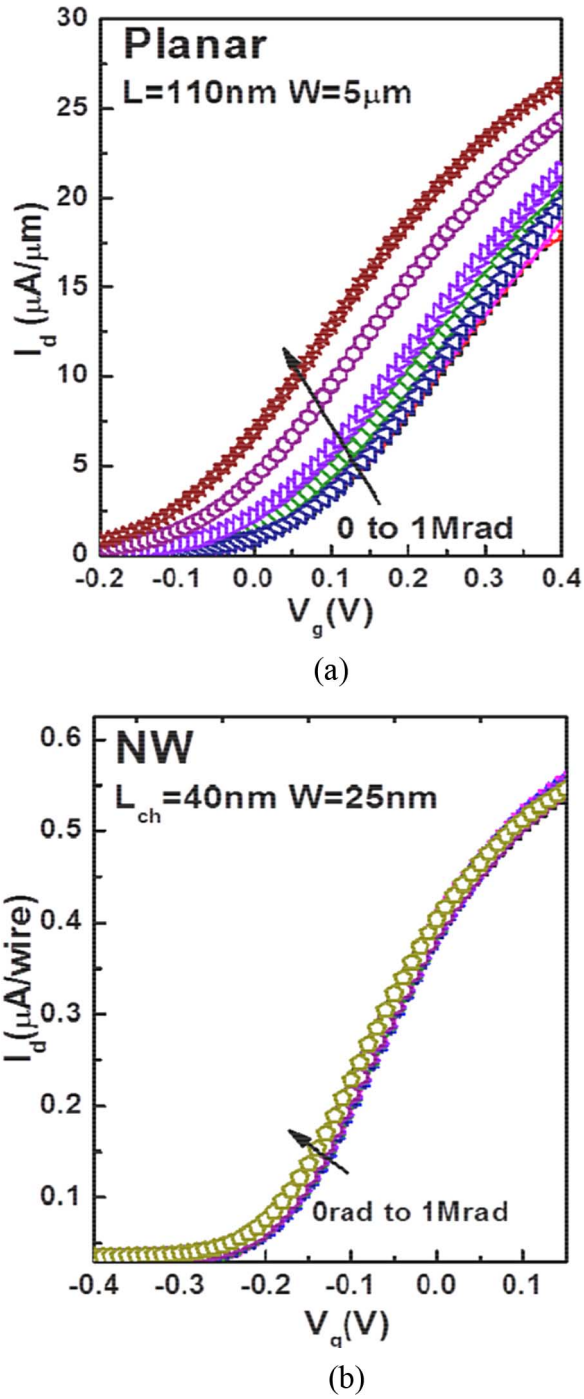

Fig. 2. $I_d - V_g$ curve shifts with increasing radiation dose up to 1 Mrad(SiO_2) for (a) planar and (b) NW InGaAs MOSFETs with all terminals grounded during irradiation.

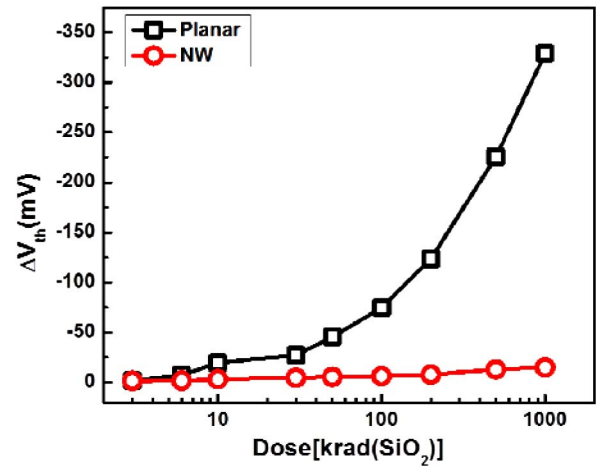

Fig. 3. Threshold voltage shifts (ΔV_{th}) as functions of x-ray dose for a planar (black) and an NW (red) InGaAs MOSFET. Both devices show negative V_{th} shifts, indicating a predominance of hole trapping.

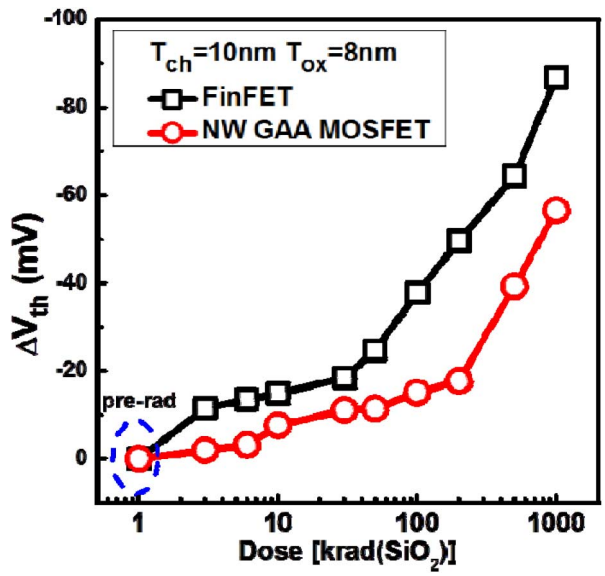

Fig. 4. ΔV_{th} as functions of x-ray exposure time for InGaAs FinFET (black) and NW GAA MOSFETs (red), respectively. The experimental uncertainty in V_{th} is approximately equal to the symbol sizes.

NW (10 nm) devices show smaller V_{th} shifts than thicker NW (20 nm) devices. Moreover, for the 10 nm NW device, V_{th} recovers to its pre-irradiation level (i.e., $\Delta V_{th} \sim 0$) shortly after the termination of the irradiation. For the thicker NW device, V_{th} recovery levels off after 100 min of room air storage. Again, very little interface-trap generation is observed.

C. TCAD Simulations

To gain a better understanding of the NW thickness dependence of the radiation hardness, we used Sentaurus TCAD to simulate the distributions of inversion electrons and electric fields in the NW devices. A 3D NW device structure was built with the same set of device configurations, such as doping level, high-k oxide thicknesses, etc, as in the real InGaAs devices. This simulation was performed using a simplified quantum mechanical model in the Sentaurus simulator, in additional to solving the usual continuity equation and Poisson equations. To match the realistic device response, surface roughness scattering and doping dependent carrier mobility models were also included in the simulations. With careful calibrations of the Sentaurus TCAD physics models, very good agreement is observed between experimental $I_d - V_g$ characteristics at a drain bias of 50 mV (black) and Sentaurus TCAD simulations in Fig. 7. The red curve shows the $I_d - V_g$ characteristic of a simulated NW device with a single wire in it, whereas there are four NWs in the actual devices studied in this work. After quadrupling the simulation result (red) of the single wire device,

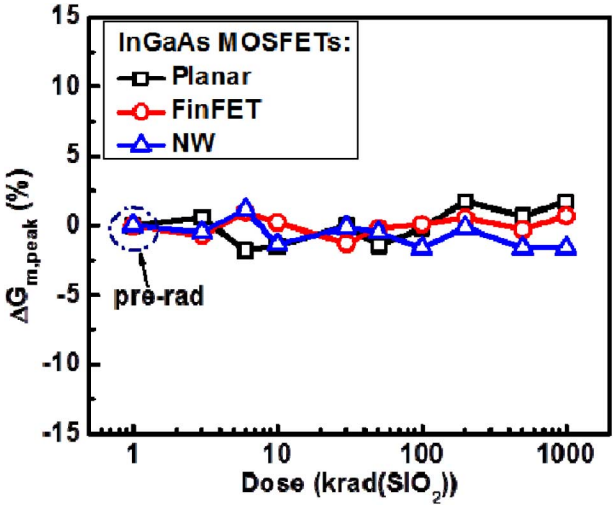

Fig. 5. Change of peak transconductance ($\Delta G_{m,peak}$) as functions of x-ray dose for InGaAs planar (black), FinFET (red), and NW (blue) MOSFETs.

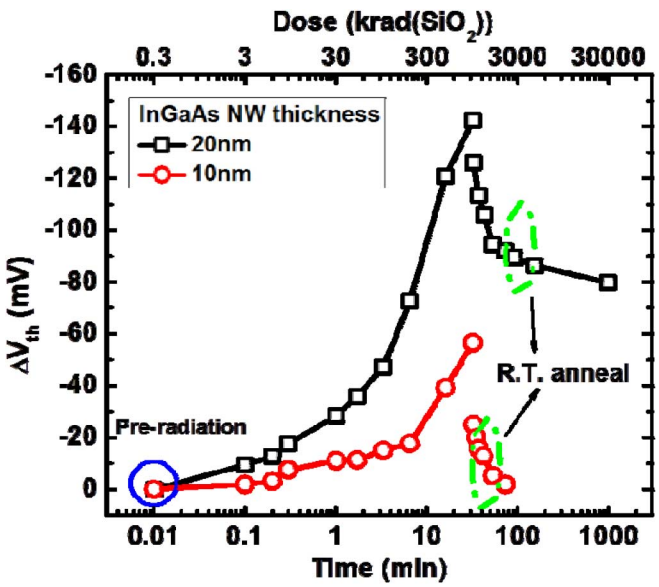

Fig. 6. ΔV_{th} as functions of x-ray exposure time for NW GAA InGaAs MOSFETs with 20 nm (black) and 10 nm (red) NW thickness, respectively. Also shown is ΔV_{th} recovery after 1 Mrad(SiO_2) dose at room temperature.

we get a good fit between simulation (blue) and experimental (black) results.

Fig. 8 shows cross-sectional views of (a) inversion electron densities and (b) electric field distributions in devices with 10 nm and 20 nm NW thicknesses. As seen in Fig. 8(a), the inversion electrons in the 20 nm-NW device are distributed more towards the surfaces than the center, in contrast to the 10 nm-NW counterpart. Fig. 8(b) shows that the electric field in the gate oxide of the 20 nm NW device is much stronger than that in the 10 nm NW device. The stronger electric-field in the gate oxide promotes separation of X-ray generated e-h pairs [8] and more rapid sweeping out of electrons, resulting in more hole trapping and larger ΔV_{th}. For 7 nm and more advanced technologies, it is also quite possible that FinFET structures may be employed, instead of GAA. Our preliminary TCAD simulations on FinFET structures (not shown) also show higher

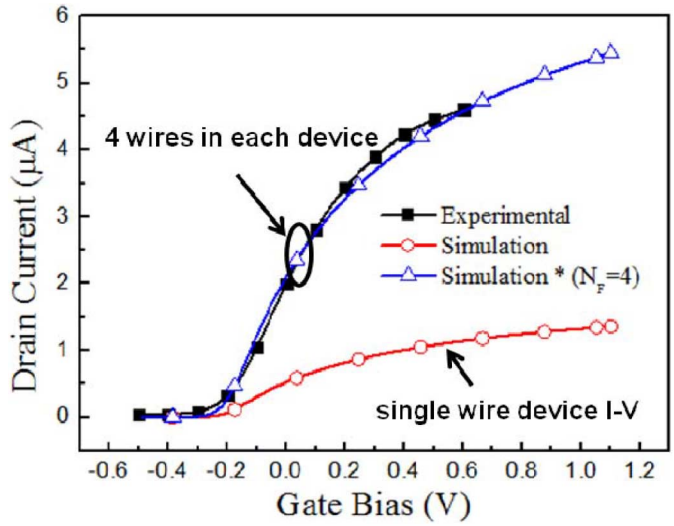

Fig. 7. Experimental $I_d - V_g$ characteristics at a drain bias of 50 mV (black) and Sentaurus TCAD simulations (blue). The red curve shows the simulated $I_d - V_g$ characteristic with a single nanowire in a device. There are four wires in each NW device studied in this work. Very good agreement is found between the TCAD model and the experimental results.

electric fields in gate oxide compared to NW MOSFETs with the same channel thickness (10 nm) and gate oxide thickness (8 nm), so trends in FinFET radiation response with similar dielectric layers should be similar to those shown here. Detailed studies of how device structure (FinFET versus gate all around) and channel shape affect radiation hardness is a fruitful topic for future work.

D. Process Effect: Forming Gas Anneal

FGA has been shown to improve $Al_2O_3/InGaAs$ interface quality by reducing interface trap density [6]. On the other hand, exposure to hydrogen during device processing can sometimes degrade MOS radiation hardness [9]–[12]. Thus, it is worthwhile to understand how FGA affects the radiation hardness of InGaAs NW devices. Fig. 9 compares the radiation hardness of NW devices with and without post-metal forming gas anneal (FGA). Again, primarily hole trapping is observed for both devices. Devices that received a FGA exhibit smaller ΔV_{th} than those without FGA. Indeed, the threshold voltage shifts of these optimized devices are nearly as small as those observed in previous studies of Si/SiO_2 nanowire devices [13], despite the III-V channel and high-k dielectric in these devices, which typically show larger defect densities than Si/SiO_2 devices [9].

Low frequency noise measurements have also been used to probe oxide trap information in NW devices with and without FGA treatment. Fig. 10 shows that for unirradiated NW devices of each type, $S_{Id}/I_d^2 - I_d$ curves (with S_{Id} being the current noise spectral density) fit a simple number fluctuation model [8], [14], [15] over a wide range of biases. Hence, S_{Id}/I_d^2 is proportional to the effective border-trap (near-interfacial oxide trap) density D_{bt}. This strongly suggests that D_{bt} in the FGA-treated device is much smaller than that in the non-FGA treated device, consistent with a reduced amount of oxide-trap charge in the FGA-annealed device in the bulk and near-interfacial region, and resulting in less threshold voltage shift. Thus, FGA not only

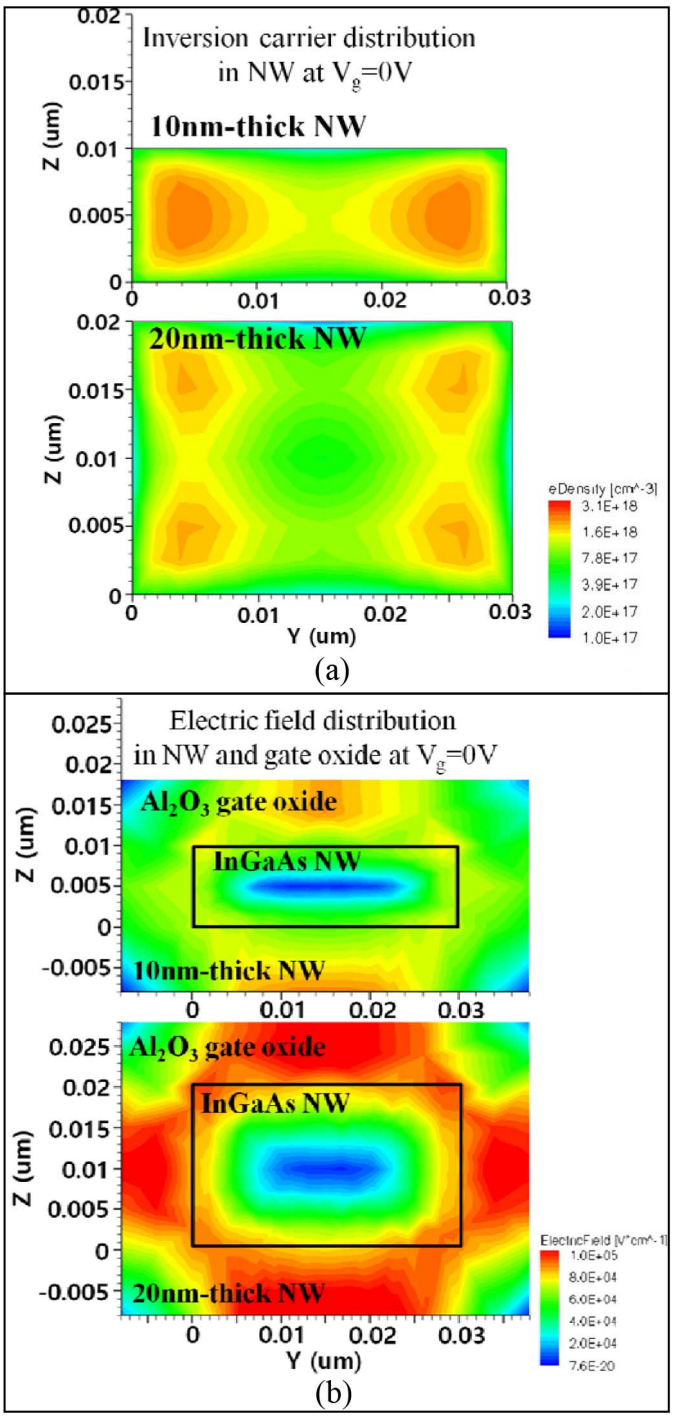

Fig. 8. TCAD simulations for $V_g = 0$ V(a) Inversion electron distribution in InGaAs NW devices with 10-nm NW thickness (upper) and 20-nm NW thickness (lower); (b) cross-sectional views of electric fields in MOSFETs with 10 nm (upper) and 20 nm of NW (lower).

benefits InGaAs device electrical performance by reducing interface trap density, but also improves its radiation hardness by reducing oxide trap density.

E. Gate Bias Effect during X-Ray Irradiation

Fig. 11 shows ΔV_{th} as functions of dose in NW GAA MOSFETs under three different gate bias conditions (i.e., grounded,

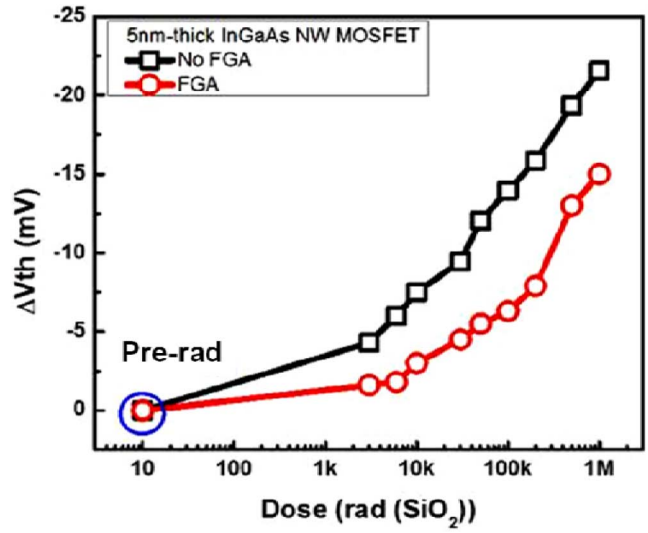

Fig. 9. ΔV_{th} as a function of dose for InGaAs NW MOSFETs with (red) and without (black) FGA.

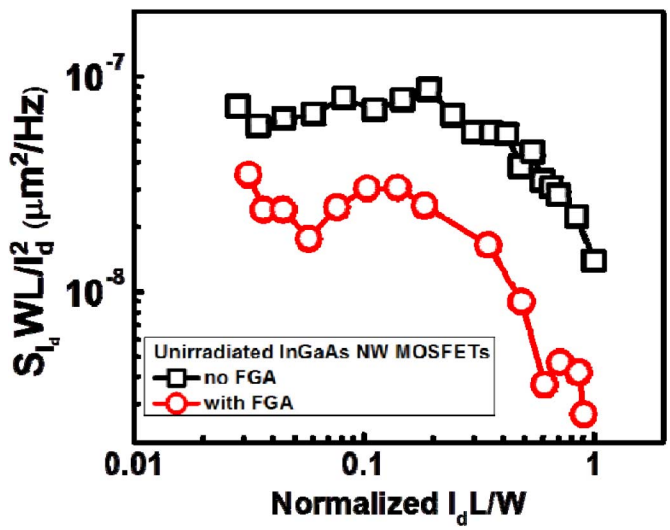

Fig. 10. Normalized $1/f$ noise measured on unirradiated devices. Higher oxide trap density is shown for the device without FGA than with FGA.

and 0.5 V above/below V_{th}). Negative gate bias (0.5 V below V_{th}) during x-ray irradiation leads to noticeably larger negative ΔV_{th} ($\sim$ 42 mV at 1 Mrad(SiO_2)) than gate grounded or positively biased irradiation. Similarly, low-frequency ($1/f$) noise scans from subthreshold to the strong inversion region indicate that irradiation under negative gate bias results in a 2X higher noise magnitude after irradiation than the case of gate grounded (Fig. 11). Again, the measured S_{Id}/I_d^2 versus I_d plots show that all three devices follow a simple number fluctuation model well [14], [15]. When good agreement between the experimentally measured noise and a simple number fluctuation model is observed, the dominant source of noise are border traps with an approximately uniform energy distribution [14]. Therefore, the results of Fig. 12 are consistent with an increase in border-trap charge density for negative bias irradiation in these devices. This result is consistent with recent results on nano-scale SiGe

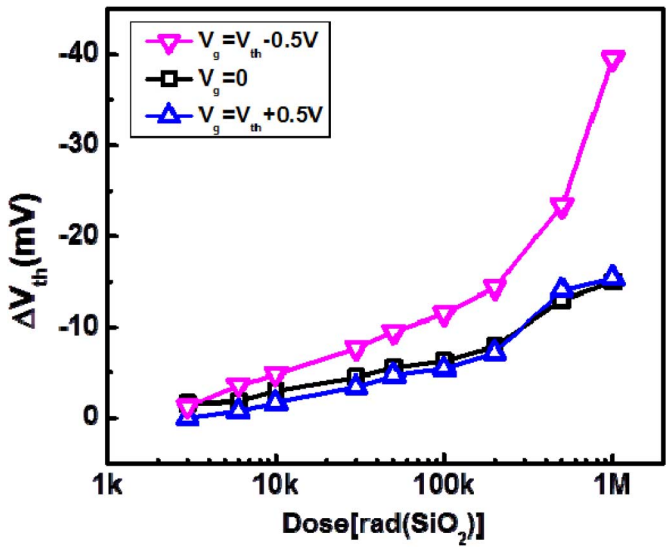

Fig. 11. ΔV_{th} as functions of radiation dose for InGaAs NW GAA MOSFETs under various gate bias conditions during radiation.

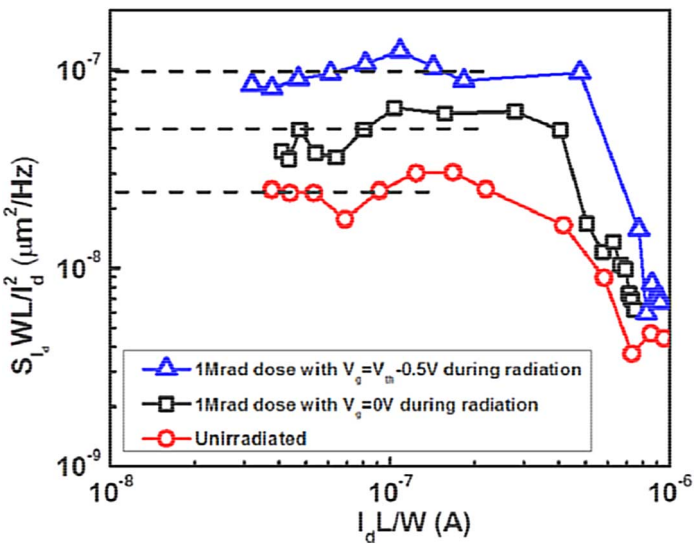

Fig. 12. Low-frequency $1/f$ noise measurements on NW GAA MOSFETs under two different bias conditions during radiation. Red circles represent data taken on an unirradiated device for comparison.

devices with high-k dielectrics, where negative bias also led to worst-case TID response [16].

IV. Conclusion

We have observed that the NW thickness, forming-gas anneal and gate bias during radiation all can significantly affect the radiation hardness of InGaAs NW GAA MOSFETs. More specifically, the thinner the NW, the better the radiation hardness. Simulations show that this is a result of the reduced electric field in the gate oxide. FGA improves device radiation hardness by reducing the border (near-interfacial oxide-trap) charge density, which was detected by low frequency noise measurement. The results illustrate that InGaAs NW GAA MOSFETs are very promising for potential future use in space applications.

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