Germanium nMOSFETs With Recessed Channel and S/D: Contact, Scalability, Interface, and Drain Current Exceeding 1 A/mm

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***Abstract*— A novel recessed channel and source/drain (S/D) technique is employed in Ge nMOSFETs, which greatly improves metal contacts to n-type Ge with contact resistance of down to 0.23 $\Omega \cdot$ mm and enhances gate electrostatic control with I_{ON}/I_{OFF} of > 10^5. The recessed S/D contacts are thoroughly investigated, showing strong dependence on the doping profile. For the first time, the drain current of Ge nMOSFETs has exceeded 1 A/mm with an I_d of 1043 mA/mm on a 40-nm L_{ch} device. Scalability study is carried out in deep sub-100-nm region on Ge nMOSFETs with L_{ch} down to 25 nm. Interface study is also conducted with a new postoxidation method introduced, which significantly reduces the interface trap density. Device behaviors corresponding to interface traps are also investigated through a Technology Computer Aided Design simulation.**

***Index Terms*— Ge, Ge-on-insulator (GeOI), MOSFET, nMOSFET, recessed channel, recessed source/drain (S/D), scalability.**

I. Introduction

WITH the continuous device scaling down as predicted by Moore's law, the Si CMOS technology is inevitably coming to an end. High mobility materials have been seriously considered and investigated in the last decade. Recently, Ge technology has been pushed for pMOSFETs, while III–V has been intensively studied for nMOSFETs because of their superior carrier mobilities. Great achievements have been made on Ge pMOSFETs, such as high quality interface with low interface traps [1]–[5], high-κ dielectric integration [3], [5]–[7], multigate structures [7]–[10], and aggressive device scaling [3], [7], [11]. However, from a manufacturing point of view, it is much more favorable to use the same material for both nMOSFETs and pMOSFETs, which could greatly reduce the process complexity, cost, and various reliability issues compared with the cointegration of III–V and Ge on the Si CMOS platform. The III–V materials, suffering from their poor hole mobilities, can hardly achieve this goal, whereas Ge, with the highest hole mobility, also has a factor of two larger electron mobility compared with Si. Benefiting from its high and balanced carrier mobilities, Ge is quite promising for post-Si CMOS technology.

However, despite recent progresses of n-type Ge in terms of effective electron mobility [3], [12]–[14] and interface passivation [1]–[3], [15], [16], realization of well-behaved Ge nMOSFETs still faces many challenges. High electron density in the channel is difficult to realize at a nonideal oxide–Ge interface, since the trap neutral level (TNL) [17]–[19] of Ge aligns near valence band edge (E_V) and the large Schottky barrier height of electrons (~0.5 eV) [17], [20]–[23] in the n-type Ge metal contacts leads to a large contact resistance.

In [24], a new recessed channel and source/drain (S/D) technique has been introduced to ameliorate the performance of Ge n-type transistors. Thanks to the low-contact resistance on n-type Ge enabled by the recessed S/D and the excellent gate electrostatic control realized by the fully depleted ultrathin body (FD-UTB) recessed channel, record high-performance Ge nMOSFETs are achieved. In this paper, we expand the previous results on Ge nMOSFETs [24] and investigate them comprehensively in the aspects of contacts, scalability, and interface. This paper is organized as follows. The device structure and experiment details are presented in Section II. Section III explains the basic working principle and electrical results of the metal contact to n-type Ge with recessed S/D. Section IV analyzes the device performance, benchmarks this paper with other published results, and studies the device scalability. Section V investigates the influence of high-κ to Ge interface on the device behaviors. Section VI compares the accumulation mode (AM) and inversion mode (IM) devices for both Ge nMOSFETs and pMOSFETs and discusses how they are affected by the E_F alignment at Ge's interface. Finally, the conclusion is given in Section VII.

II. Experiment

The Ge-on-insulator (GeOI) substrate used in this paper consists of 180-nm (100) Ge layer, 400-nm SiO_2 buried oxide layer, and a (100) Si handle wafer grown by the Smartcut technology from Soitec. Fig. 1(a) shows the device structure with the recessed channel and S/D highlighted.

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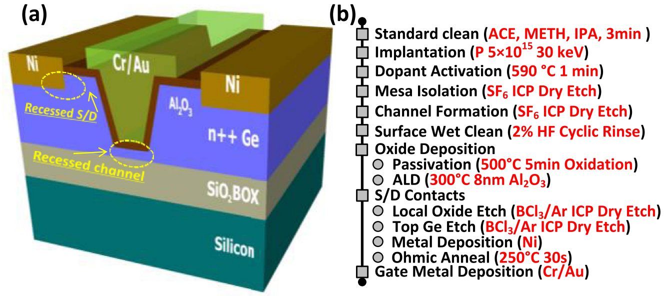


Fig. 1. (a) Device schematic. Yellow dashed circles: recessed channel and S/D are highlighted. (b) Key processes in the fabrication of the Ge recessed channel and S/D nMOSFET.

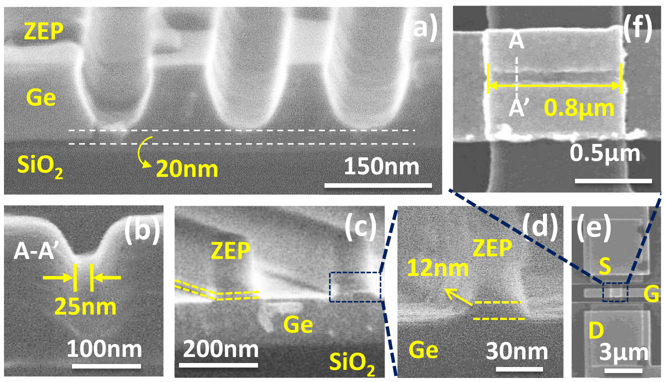


Fig. 2. (a) Test recessed channels, T_{ch} is 20 nm. (b) Shortest 25-nm L_{ch} recessed channel after ALD growth, the Al_2O_3 could be clearly observed. (c) Test recessed S/D structure. (d) Zoomed-in view of the etched area, 12-nm Ge is removed. (e) Top–down view of a fabricated device. (f) Zoomed-in view of the gate area in (e). The W_{ch} is 0.8 μm.

Fig. 1(b) briefly summarizes the fabrication processes in this experiment. After standard cleaning, the sample was first globally implanted with phosphorus ions, followed by an ion activation. Then, the device isolation was performed by a dry etching process. The channel region was defined by electron beam lithography, and an optimized SF_6 Inductively Coupled Plasma (ICP) dry etching with a high aspect ratio was used for the recessed channel formation. By precisely controlling the etching time, a desired channel as thin as 20 nm was realized, as shown in Fig. 2(a). The smallest channel length (L_{ch}) realized is 25 nm, as shown in Fig. 2(b). Surface wet cleaning was then applied to fix the surface damage induced by the dry etching. Next, the sample was immediately transferred into an oxidation furnace for GeO_x growth as the interface passivation. The GeO_x layer is confirmed to be ~3 nm by C–V measurement. Following oxidation, the sample was transferred into an atomic layer deposition (ALD) chamber for 8 nm of Al_2O_3 high-κ dielectric deposition. After etching away the oxides in the S/D region, an ICP dry etching was used to remove the top Ge layer of several nanometers as the recessed S/D etching, which is one of the key processes in this experiment. Here the BCl_3/Ar dry etching was carefully calibrated to precisely control the etching rate, which is ~15 nm/min. About 12-nm of Ge layer was removed in this procedure, as shown in Fig. 2(c) and (d). Note that different etching times were used to study the dependence of contact resistance on the recessed depth (D_r), which is discussed in Section III in detail. The 100-nm Ni was then deposited as the S/D contact metal, followed by an ohmic anneal. Finally, Cr/Au was deposited as the gate metal.

Fig. 2(e) shows a fabricated device and its channel area is enlarged in Fig. 2(f). The fabricated nMOSFETs have a channel width (W_{ch}) of 0.8 μm, a channel thickness (T_{ch}) of 20 nm, and L_{ch} from 25 to 100 nm. The gate dielectric is composed of 3-nm GeO_x and 8-nm Al_2O_3, corresponding to an equivalent oxide thickness (EOT) of 5.2 nm. The width of the metal contact is 3.5 μm.

III. Ohmic Contacts on n-Type Ge

A. Basic Principles

The charge neutrality level (CNL) and the Fermi level (E_F) pining are fundamental properties of metal to semiconductor interface. The CNL of Ge is located about 0.1 eV above E_V [17], [23] and the pining factor (S) has been experimentally calculated by various reports [17], [21] to be ~0.05. There is almost no metal work-function modulation to the Schottky barrier of metal–Ge contact. The Fermi-level pining of Ge near the CNL leads to a large barrier height ($q\Phi_{\text{B,e}}$) for electrons but small barrier height ($q\Phi_{\text{B,h}} = E_{\text{g,Ge}} - q\Phi_{\text{B,e}}$) for holes. Thanks to the low $q\Phi_{\text{B,h}}$, ohmic contacts to p-type Ge is quite easy to achieve. Moreover, the low diffusivity and high electrical activation efficiency with doping density (N_D) of up to 6.6×10^{20} cm^{-3} [25] of the p-type ions (such as B, BF_2, and Ga) in Ge could acquire low resistivity contacts and ultrashallow junctions, which, combined with the highest hole mobility, make Ge the ideal p-type candidate to replace Si.

However, the high barrier of electrons in Ge makes the metal contact to n-type Ge like a Schottky diode, rather than the ohmic contact to p-type Ge. Furthermore, the n-type dopants of Ge, such as P and As, show low activation efficiency and the maximum activated doping concentration has been reported in the range of 5×10^{19}–1×10^{20} cm^{-3} [30], making the resistivity of n-type contact to Ge larger. Recently, some studies [20]–[22], [26] have successfully demonstrated well-behaved n-type ohmic contact by inserting a passivation layer between metal and Ge to minimize the gap states, unpinning E_F to lower the Schottky barrier. However, it is a challenge to integrate this process into standard CMOS technology process and no results have been reported at the transistor level.

In principle, there are two types of approaches normally used to obtain an ohmic contact to semiconductors: 1) lowering the barrier height and 2) decreasing the barrier width (W_{SB}). On the condition of the strong Fermi-level pining in Ge, the simple but effective recessed S/D method adopted here is to optimize the contact by lowering W_{SB}. Fig. 3 explains the mechanism of the contact improvement in the recessed S/D structure. The profile of doping ions inside a semiconductor can be approximated by a Gaussian distribution function [27], as shown in the ion concentration (N_D) versus depth relation. The peak of the ion distribution is located several nanometers beneath the surface instead of at the surface. Accordingly, the N_D first increases and then deceases rapidly along the depth axis from the surface to the peak

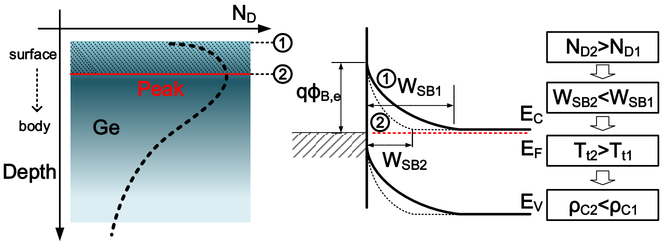


Fig. 3. Contact improvement mechanism in the recessed S/D structure. Higher surface doping leads to higher tunneling efficiency of electrons through the barrier, thus lowering the resistivity.

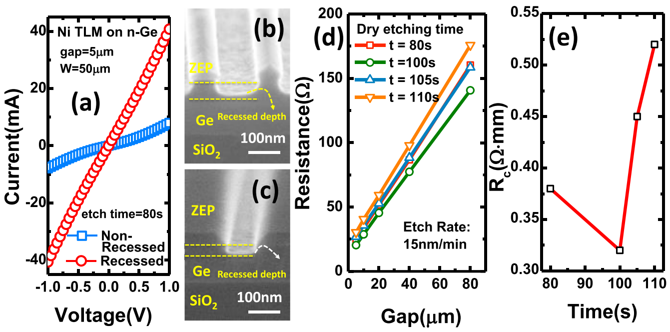


Fig. 4. (a) I–V curves of two top TLM contacts on n-type Ge with and without the recessed S/D for Ni. (b) and (c) Testing recessed S/D structures with different recessed depths. (d) TLM results of recessed contacts on n-type Ge with different recessed depths (etching time). (e) Contact resistance dependence on the etching time.

location, then to deep inside Ge. By etching away the top less doped layer above the peak position, the N_D in the newly formed surface region can be pushed much higher than before. The Schottky barrier width is then significantly reduced, as shown in the band diagram. It further significantly enhances the electron tunneling current through the barrier, thus the contact resistance is greatly reduced. For the ion implantation condition used in this paper, the peak is ∼30 nm away from the surface [27], [28].

B. Results and Discussion

Testing structures indicate that the recessed S/D process removed about 12 nm of top Ge layer, shown in Fig. 2(d) and (e). Fig. 4(a) shows the I–V curves of two top square TLM contacts with $W_{\text{TLM}} = 50\ \mu$m and a gap of 5 μm using Ni with and without the recessed S/D. Great enhancements (current improvement of more than ×5) are observed and the recessed S/D contact behaves in ohmic.

The contact resistivity is strongly correlated with the doping density at the surface of Ge. Recessed contacts on n-type Ge with various recessed depths are studied, as shown in the SEM images of testing recessed S/D structures in Fig. 4(b) and (c). As determined by the ion implantation, different D_r used would result in different doping concentration at the newly formed surface defined by dry etching, which is confirmed experimentally in Fig. 4(d). Four recessed S/D TLM contacts with different dry etching time are used to extract R_c and R_{sh}. The R_{sh} shows very small variations as indicated by the slopes of the lines. However, the R_c changes prominently as proved by the different y-axis intercepts. Fig. 4(e) provides the R_c versus etching time (or D_r) relationship, demonstrating that R_c first decreases

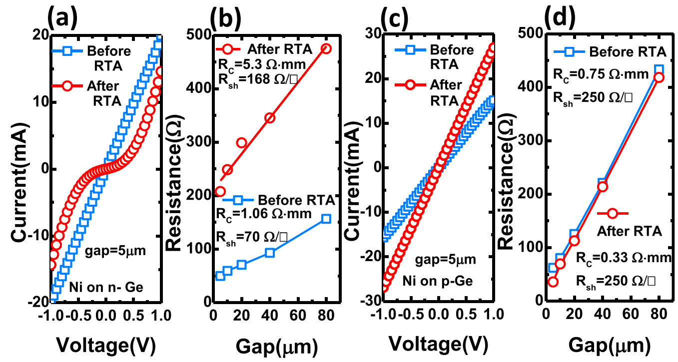


Fig. 5. (a) I–V curves of same two top Ni TLM contacts on n-type Ge with recessed S/D before and after RTA in linear scale. (b) TLM results of the same TLM contacts in (a). (c) I–V curves of same two top Ni TLM contacts on p-type Ge with recessed S/D before and after RTA in linear scale. (d) TLM results of the same TLM contacts in (c).

and then increases with larger D_r. It is related with the doping profile inside Ge, as shown in Fig. 3. The N_D at the new surface first increases and then decreases rapidly with deeper etching, resulting in varying Schottky barrier widths, thus different R_c. Therefore, there is an optimal recess time or depth for low resistivity ohmic contacts. By carefully calibrating the etching time, the lowest contact resistance we have achieved in this paper is 0.23 $\Omega \cdot$ mm and the contact resistivity is $\sim 5 \times 10^{-6}\ \Omega \cdot \text{cm}^2$.

To further study the thermal stability of the recessed S/D contact, thermal annealing was conducted after the fabrication and electrical measurements and the contacts were annealed at 350 °C for 30 min in forming gas ambient by Rapid Thermal Annealing (RTA). Fig. 5(a) shows the I–V curves of same two Ni TLM contacts on n-type Ge with the recessed S/D before and after RTA. After the long-time annealing, the ohmic contact changes to Schottky contact and the conducting current degrades. The TLM data of the same TLM contacts are given in Fig. 5(b). The R_c increases significantly from 1.06 to 5.28 $\Omega \cdot$ mm and R_{sh} degrades from 70 to 168 Ω/□. To examine the physics accounting for this phenomenon, recessed S/D contacts on p-type Ge were also processed and treated in RTA with the same condition, as provided in Fig. 5(c) and (d). On the contrary, the R_{sh} remains the same but R_c improves from 0.75 to 0.33 Ω/□ after annealing.

The distinctive difference between effects of annealing on n-type and p-type contacts could be traced to the doping ion distribution inside Ge. As already mentioned, the n-type doping ions (P, As, and Sb) inside Ge have low activation efficiency but high diffusivity. The recessed S/D is introduced to improve the doping density at the surface to overcome the low activation efficiency issue. However, due to high diffusivity, the long-time annealing would act as the drive in process, which is commonly used in thermal diffusion. After annealing, the peak of P ion concentration moves further into the Ge body and the P ions distribute more uniformly inside Ge, leading to a less doped surface region and lower peak doping concentration. Less doped surface region leads to rapidly increasing R_c and lower doping density increases the R_{sh}. However, the p-type doping ions (B, BF_2, and Ga) have

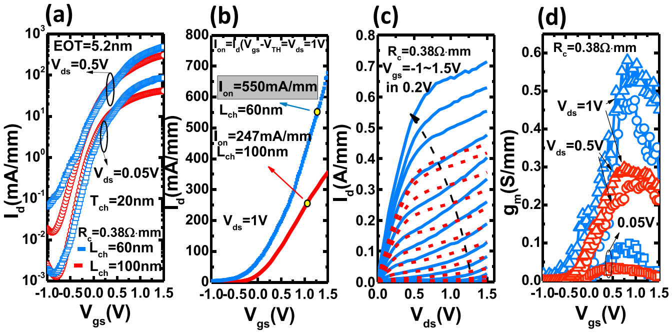


Fig. 6. (a) Transfer curves of two Ge nMOSFETs with $L_{\mathrm{ch}} = 60$ and 100 nm at $V_{\mathrm{ds}} = 0.05$ and 0.5 V and V_{gs} from -1 to 1.5 V. (b) Transfer curves of the same two devices in (a) at $V_{\mathrm{ds}} = 1$ V in linear scale. (c) Output characteristics of the same two devices in (a) with V_{ds} sweeping from 0 to 1.5 V. (d) g_m versus V_{gs} relationships of the same two devices in (a) with various V_{ds}.

high activation efficiency and very low diffusivity. Resulted from the higher activation efficiency of BF_2 and very low Schottky Barrier Height (SBH), the R_c of p-type contacts is better than that of n-type contacts. Furthermore, due to the low diffusivity of BF_2 in Ge, the long-time annealing could not greatly redistribute the doping profile of BF_2 inside Ge, resulting in a constant R_{sh} before and after RTA. Meanwhile, Ni diffuses and reacts with Ge, leading to a lower resistivity NiGe alloy. The improvement in p-type contact indicates that the deterioration of n-type contacts is not related with the contact metal degradation, further validating the explanation based on doping profile distribution.

IV. Device Performance and Scalability

Since the channel and S/D regions of the nMOSFET here are homodoped with P, the Ge nMOSFETs here are majority carrier devices, working in AM.

A. Device Characteristics

The contact resistance of this sample is extracted to be 0.38 $\Omega \cdot$mm by TLM and the gate leakage current is on a low level of 10^{-5} mA/mm. Fig. 6(a) compares the transfer curves of two typical Ge nMOSFETs in log scale with different L_{ch} of 60 and 100 nm at $V_{\mathrm{ds}} = 0.05$ and 0.5 V. Thanks to the lightly doped channel determined by the doping profile and superior gate electrostatics control realized by the ultrathin recessed channel, the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio of the 60-nm L_{ch} device at $V_{\mathrm{ds}} = 0.05$ V is $\sim 10^5$, which is one of the largest value reported on Ge nMOSFETs. For the longer channel device, the smaller $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio is mainly attributed to poorer ON-state current in longer channel. But it has a better subthreshold slope (SS) of 185 mV/decade and better OFF-state current. The lowest SS obtained is 117 mV/decade (not shown), corresponding to a midgap D_{it} of 4×10^{12} eV^{-1}cm^{-2}, indicating a decent interface passivated by high-temperature oxidation. The threshold voltages (V_{TH}) of the two devices are linear extrapolated at a low V_{ds} of 0.05 V to be $\sim$0.2 V, indicating the enhancement-mode operation. For the ON-state characteristics, Fig. 6(b) gives the transfer curves at $V_{\mathrm{ds}} = 1$ V of the same two devices in linear scale. The near-linearly increasing I_d in high V_{gs} and V_{ds}

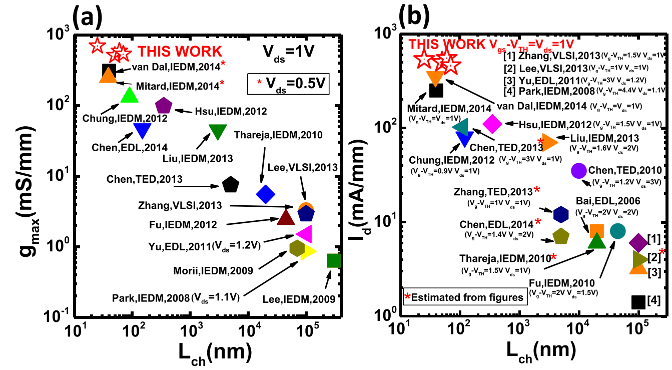


Fig. 7. (a) Drain current benchmarking of the Ge nMOSFETs in this paper with other published results. (b) Maximum transconductance benchmarking of the Ge nMOSFETs in this paper with other published results.

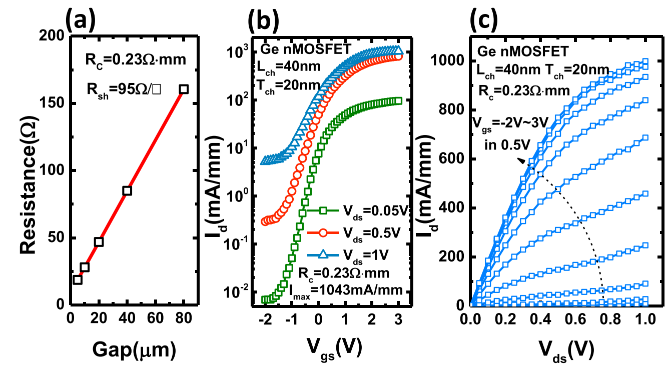


Fig. 8. (a) TLM results with the lowest R_c of 0.23 $\Omega \cdot$ mm obtained. (b) Transfer curves of a Ge nMOSFET with L_{ch} of 40 nm and T_{ch} of 20 nm with V_{gs} ranging from -2 to 3 V at various V_{ds}. (c) Output characteristics of the same device in (b) with V_{ds} from 0 to 1 V and V_{gs} from -2 to 3 V in 0.5 V step.

region indirectly proves the low-contact resistance enabled by the recessed S/D. The 60-nm L_{ch} device has a large ON-current (I_{ON}) of 550 mA/mm at $V_{\mathrm{ds}} = V_{\mathrm{gs}}–V_{\mathrm{TH}} = 1$ V.

Fig. 6(c) compares the output characteristics of the same two devices in Fig. 6(a). Both of the two devices show good pinchoff characteristics and the maximum drain current ($I_{\max}$) of the 60-nm L_{ch} device is 714 mA/mm at $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 1.5$ V. Fig. 6(d) shows the transconductance (g_m) versus V_{gs} of the same two devices in Fig. 6(a). A record high maximum g_m ($g_{\max}$) of 590 mS/mm for Ge nMOSFETs is achieved in the 60-nm L_{ch} device at $V_{\mathrm{ds}} = 1$ V. Correspondingly, the peak field-effect mobility is estimated to be 180 cm^2/Vs.

Fig. 7(a) and (b) benchmarks the I_d and $g_{\max}$ in this paper with other published results [2], [3], [9], [12], [14], [22], [29]–[39] before the publication of [24]. The Ge nMOSFETs are first scaled down to the sub-100-nm region. Breakthroughs of high-performance Ge nMOSFETs have been achieved. The I_d and $g_{\max}$ demonstrated here are comparable with the results of the well-studied Ge pMOSFETs [7], [10], revealing a promising future of full CMOS logics built solely on Ge.

As mentioned in Section III, by carefully calibrating the D_r of recessed S/D contacts, lowest R_c of 0.23 $\Omega \cdot$ mm is realized, as shown in Fig. 8(a). By integrating the low resistivity contacts, together with reduced EOT of 3.5 nm and L_{ch} of 40 nm, the performance of Ge nMOSFETs is further improved. Fig. 8(b) shows the transfer curves of

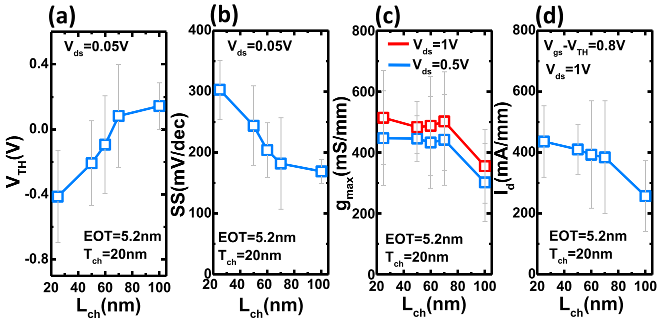


Fig. 9. (a) V_{TH} scaling trend, the V_{TH} is linearly extrapolated at a low V_{ds} of 0.05 V. (b) SS ($V_{ds} = 0.05$ V) scaling metrics. (c) g_{max} scaling trend with $V_{ds} = 0.5$ and 1 V. (d) Drain current scaling metrics with V_{gs}–$V_{TH} = 0.8$ V and $V_{ds} = 0.5$ V. Error bars: standard deviation of the measurement over ten devices at each data point.

a Ge nMOSFET with L_{ch} of 40 nm and T_{ch} of 20 nm. Thanks to the thinner EOT and T_{ch}, the device still maintains good I_{ON}/I_{OFF} ratio of more than 10^4 at low V_{ds} bias in aggressively scaled sub-50-nm channel length. Most importantly, the maximum current reaches 1043 mA/mm at $V_{ds} = 1$ V and $V_{gs} = 3$ V. The output curves of the same device are given in Fig. 8(c). It is the first time that the drain current of Ge nMOSFETs has exceeded 1 A/mm.

B. Scalability Study

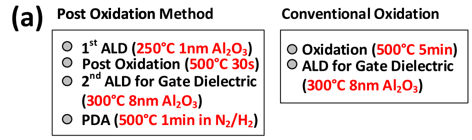
Fig. 9(a) and (b) shows V_{TH} and SS scaling metrics for Ge recessed channel and S/D nMOSFETs with various channel lengths. With a well-engineered gate-stack, V_{TH} for the long channel device ($L_{ch} = 80$ and 100 nm) is >0 V. A positive V_{TH} for the nMOSFET is the key to well-behaved CMOS applications but difficult to achieve in AM device, which requires an extra negative gate bias to fully deplete the channel. With decreasing L_{ch}, the V_{TH} rolls off and SS degrades, resulted from the stronger short channel effects (SCEs). Better SCE immunity could be obtained by further EOT scaling down, thinning the channel, better interface engineering and 3-D multigate structures. Fig. 9(c) and (d) provides the ON-state performance (g_{max}, I_d) scaling trends of Ge nMOSFETs. The g_{max} and I_d first increase but tend to be saturated with decreasing L_{ch}, which could be resulted from velocity saturation or ballistic transport.

V. Impact of Interface Quality

In Ge MOSFETs, the quality of high-κ to Ge interfaces plays a critical role. Among all of the passivation techniques, GeO_2 is demonstrated to be able to sufficiently passivate the Ge MOS interface with low D_{it}. It is promising to serve as the interfacial layer between high-κ and Ge. Here, we studied the Ge interface by both experiment and simulation.

A. Improved Interface by Post Oxidation

The EOT of gate dielectrics treated by conventional thermal oxidation is difficult to scale down because of the thick GeO_2 grown [3], [40]. To further improve the interface quality and scale down the gate oxide, a plasma postoxidation (PPO) technique has been introduced and



(b)

	Passivation	T_{ch}	Recessed S/D	Gate metal
Sample I	With Post Oxidation	20 nm	110s dry etch	Ni/Au
Sample II (as in Section II)	W/O Post Oxidation	20 nm	80s dry etch	Cr/Au

Fig. 10. (a) Differences between the PO technique and the conventional oxidation method. (b) Experimental condition differences between the devices with PO here (Sample I) and the previously reported results in Sections II and IV (Sample II).

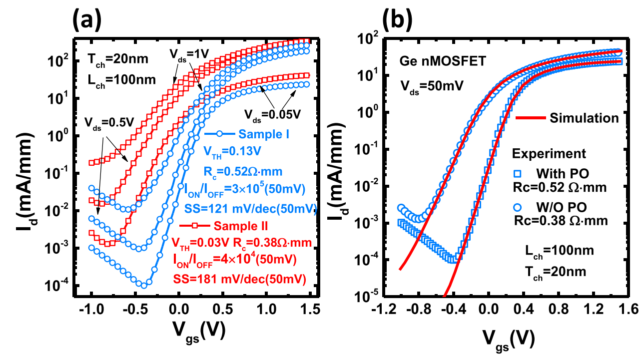


Fig. 11. (a) Transfer curves of two 100-nm L_{ch} nMOSFETs with and without the PO. (b) Experimental and simulated transfer curves of Ge nMOSFETs with and without PO in (a) at $V_{ds} = 0.05$ V.

shows promising results [3]. Nevertheless, the use of O_2 plasma to oxidize the Ge interface makes the PPO method quite complicated. In this paper, a simple PO technique is applied to improve the interface quality and reduce the EOT.

The fabrication process of the sample with PO is similar to that described in Section II except the adoption of the PO method. Fig. 10(a) compares the differences of PO technique and the conventional oxidation method. After the surface wet cleaning, 1-nm of Al_2O_3 was deposited at 250 °C by ALD as the capping layer. Next, PO was carried out in 500 °C for 30 s in pure oxygen ambient. Following this, the sample was immediately transferred to the ALD chamber for 8-nm Al_2O_3 deposition in 300 °C. Then the sample was annealed in forming gas ambient at 500 °C for 1 min as the postdeposition annealing. The process differences between the sample with PO (Sample I) and the sample without PO (Sample II, as in Section II) are listed in Fig. 10(b).

Samples I and II have a T_{ch} of 20 nm and an EOT of ∼5 nm and the differences of Sample I from Sample II are: 1) new PO for interface passivation; 2) larger recessed S/D depth; and 3) higher work function Ni/Au gate metal. Because of the dependence of R_c on recessed depth, which is explained in Section III, the contact resistance of Sample I is extracted to be 0.52 Ω·mm. Fig. 11(a) compares the transfer curves of two 100-nm L_{ch} devices in Sample I and II. The device in Sample I has: 1) a much steeper SS of 121 mV/decade, a higher I_{ON}/I_{ON} ratio, and a smaller drain-induced barrier lowering, indicating enhanced gate control from the better interface quality by the PO technique; 2) a positively shifted V_{TH}, which could be due to the larger Φ_{ms} from the Ni/Au gate metal; and 3) reduced drain current, due to the shift of V_{TH} and larger contact resistance.

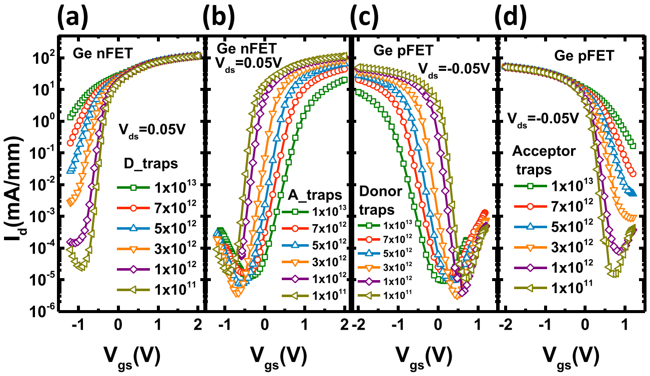


Fig. 12. Simulated transfer curves at $|V_{ds}| = 0.05$ V. (a) Ge nMOSFET with different donor-type interface trap densities. (b) Ge nMOSFET with different acceptor-type interface trap densities. (c) Ge pMOSFET with different donor-type interface trap densities. (d) Ge pMOSFET with different acceptor-type interface trap densities.

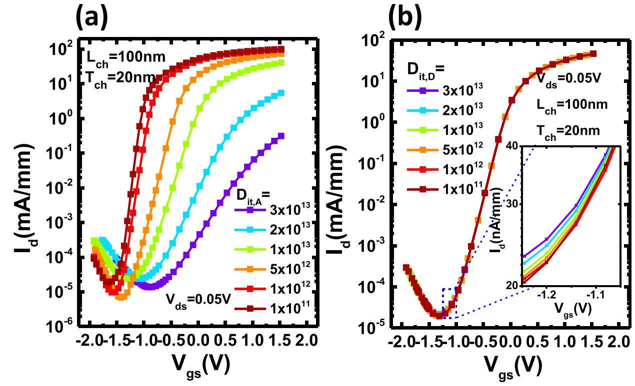


Fig. 13. (a) Simulated transfer curves of Ge nMOSFET with different acceptor trap densities at $V_{ds} = 0.05$ V. (b) Simulated transfer curves of Ge nMOSFET nFET with different donor trap densities at $V_{ds} = 0.05$ V. Inset: enlarged transfer curves in device OFF-state.

To better examine the interface, Technology Computer Aided Design (TCAD) simulation is carried out to fit the experimental curves by Synopsys Sentaurus Device, considering the interface trap models. Since Ge is widely reported to have an acceptor-dominant interface [4], [17], [23], only the acceptor trap is considered here. The acceptor traps are placed from the TNL ($\sim$0.1 eV above E_V) to the conduction band edge (E_c) uniformly. Fig. 11(b) shows the simulated and experimental transfer curves of the 100-nm L_{ch} devices with and without PO in Fig. 11(a). By fitting the experimental data using simulation, the interface trap densities are extracted to be 3×10^{12} and 9×10^{12} cm^{-2}eV^{-1} for samples with and without the PO, respectively, confirming an improved interface by the PO technique [41].

B. Effects of Acceptor and Donor Traps to Device Behaviors

For more comprehensive analysis, donor traps are further added into the simulation with the same setup described previously. The interface traps are set to distribute throughout the bandgap uniformly. The acceptor traps are neutral when empty and negatively charged when ionized (capture an electron), while the donor traps are neutral when filled and positively charged when ionized (lost an electron).

Fig. 12(a) shows the simulated transfer curves of nMOSFETs with different donor-type interface trap densities ($D_{it,D}$). With increasing $D_{it,D}$, the ON-state performance remains unchanged but the OFF-state performance degrades. It affects the nMOSFETs' characteristics in three ways: 1) negatively shifted V_{TH}; 2) degraded SS; and 3) increased OFF-state current. It is related with ionization of donor traps with different E_F alignments. In device ON-state, E_F is located near E_C and all the energy levels below E_F are filled with electrons. Thus, almost all the donor traps are neutral. Therefore, the ON-state performance remains the same. However, when negative gate bias is being applied to turn OFF the device, the E_F is moving down from E_C to E_V, making more and more donor traps above E_F ionized and building up positive net charge at the interface. The positive charge acts as a positive voltage biased to the gate, consuming the negative gate bias applied to turn OFF the device and shifting V_{TH} negatively. The electron capturing and releasing process of these traps further affects the response of carriers to gate voltage, thus degrades the SS. Therefore, the OFF-state performance is deteriorated.

Fig. 12(b) gives the device response to the acceptor-type interface trap densities ($D_{it,A}$). It is found that increasing acceptor trap density would also greatly affect the device in three different ways: 1) positively shifted V_{TH}; 2) degraded SS; and 3) reduced ON-state current. In device OFF-state, E_F is close to E_V. Majority of the acceptor traps are located above E_F and empty, remaining neutral. Thus, the OFF-state performance remains unchanged. Whereas, with increasing V_{gs} bias, more and more electrons are captured by acceptor traps, building up negative net charge at the interface, shifting the V_{TH} positively. The negative charge limits the electron accumulation and thus reduces the drive current. The acceptor traps would also affect the response of carriers to gate bias, and hence degrades SS. Moreover, severer Coulomb scattering would be introduced by the ionized traps, which would degrade the mobility.

However, the responses of pMOSFET to these two types of interface traps are on the contrary to those of nMOSFETs. Fig. 12(c) shows the transfer curves of pMOSFETs with different $D_{it,D}$. Because E_F in pMOSFET's OFF-state is located near E_C, majority of the donor traps are filled and neutral, thus the OFF-state performance is not affected. When negative voltage is applied to turn ON the device, E_F moves from E_C down to E_V, making more and more donor traps ionized and building up net positive charge at the interface. Thus, the V_{TH} is shifted negatively. Similar to the case of acceptor traps to nMOSFETs, the SS and ON-state performance would be degraded. In Fig. 12(d), the situation of acceptor traps to pMOSFETs is the same as that of donor traps to nMOSFETs.

In real devices, the trap distribution should be considered. The acceptor traps are modeled to distribute above the TNL and donor traps are located beneath TNL [17]–[19]. The TNL is a fundamental property of semiconductor to oxide interface. The location of TNL is different in different materials. For Ge, the TNL is located

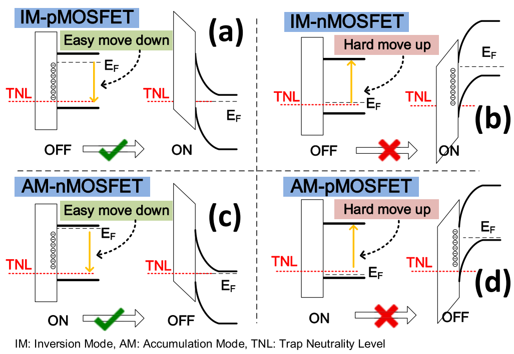


Fig. 14. Band diagrams in device ON-state and OFF-state and the correlations between EF and the TNL of Ge (a) IM pMOSFET, (b) IM nMOSFET, (c) AM nMOSFET, and (d) AM pMOSFET.

about 0.1 eV above E_V [17], [23] with a nonideal oxide–semiconductor (OS) interface, which indicates that the interface of Ge is mainly acceptor dominated. TCAD simulation is further conducted with the modified trap distribution. The acceptor traps are set to be located from TNL to E_c and donor traps distribute from TNL to E_v.

Fig. 13(a) and (b) shows the transfer curves of Ge nMOSFET with different $D_{\mathrm{it},A}$ and $D_{\mathrm{it},D}$, respectively. For Fig. 13(a), same as in Fig. 12(a), the device performance is mainly limited by the acceptor traps which almost distributes throughout the bandgap. That is why high inversion electron concentration is very hard to achieve in Ge nMOSFET. For donor traps in Fig. 13(b), positive charge is built up when E_F moves below the TNL, preventing E_F from further moving down to E_V. Thus, it degrades the OFF-state performance, as shown in the inset figure. However, most of the donor traps are located below the E_F and are neutral. Therefore, the net charge contributed by donor traps at the interface is almost zero. Hence, their influence to the Ge nMOSFET is negligible.

For Ge pMOSFET operation, E_F is located near E_V and close to the TNL in the inversion regime. Thus, most of the donor traps below E_F are empty and neutral. Most importantly, majority of acceptor traps which dominate the Ge interface distribute above E_F and are also empty and neutral. Therefore, there is almost no net charge built up in the ON-state.

VI. Effect of E_F Alignment to Device Behavior

For a nonideal OS interface, the E_F at the interface tends to be aligned near the TNL due to the charges induced by ionized traps. As stated in Section V, the TNL of Ge is ~0.1 eV above E_V. Due to the instable nature of Ge's native oxide (GeO_x), the high-κ to Ge interface is a big challenge for a long time. Although there have been great advancements in optimizing Ge's interface [3], [4], [6], the interface quality of Ge is still not easy to reach the quality of Si/SiO_2 interface and E_F cannot be freely moved due to the existence of large amount of interface traps. In such circumstances, new approaches which could overcome the interface problems are needed.

Fig. 14 explains the interactions between E_F and the TNL in four types of Ge MOSFETs.

1) For the conventional Ge IM pMOSFET in Fig. 14(a), the channel is n-doped and E_F is located in the conduction band side in the flat-band condition. The negative charges built up by ionized acceptor traps below E_F would act as a negative gate bias and pull E_F down to the TNL and close to E_V. In this case, E_F tends to move down from E_C to E_V to switch from OFF- to ON-state and it is easy to realize high inversion carrier concentration to get high drain current. This band alignment helps to make high-performance Ge IM pMOSFETs.
2) However, for the conventional Ge IM nMOSFET in Fig. 14(b), the channel is p-doped and E_F is initially near E_V. When E_F is pulled up by positive gate bias to turn ON the device, more and more acceptor traps are ionized, building increasing negative charge at the interface, which prevents E_F from further moving up and limits the inversion of minority carriers (electron). Hence, it is difficult to move E_F fully up to E_C and realize high inversion carrier density. That is the reason that Ge IM nMOSFETs are severely limited by the interface traps and high drain current is difficulty to obtain.
3) On the contrary, for the Ge AM nMOSFET shown in Fig. 14(c), its channel is n-doped as the IM pMOSFET. It is easy to achieve high accumulation carrier (electron) density since the bulk E_F is initially close to E_C and a small increase of E_F would make the number of accumulating electron exponentially increase. Moreover, the build-in negative charge by ionized acceptor traps assists the E_F to move down to switch the device OFF. That is why high drive current and high $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio are realized in the Ge AM nMOSFETs in this paper.
4) The Ge AM pMOSFET in Fig. 14(d) is similar to the case of the Ge IM nMOSFET. It is difficult to move E_F up to E_C to switch the device from ON- to OFF-states in the p-doped channel due to the negative charge from ionized acceptor traps.

From the analysis above, for Ge, only IM pMOSFETs and AM nMOSFETs could work well in all of the four types of devices (IM pMOSFET, IM nMOSFET, AM pMOSFET, and AM nMOSFET), considering the nonideal OS interface. For the Ge MOSFET with a defective acceptor-dominant interface, n-type doped channel can be used for both AM nMOSFETs and IM pMOSFETs.

VII. Conclusion

We have demonstrated a novel recessed channel and S/D technique for the Ge CMOS technology development. The Ni contacts on n-type Ge with recessed S/D provides great improvement over nonrecessed ones, showing an ideal ohmic behavior with R_c as low as 0.23 $\Omega \cdot$ mm. Sub-100-nm Ge nMOSFETs with T_{ch} of 20 nm and L_{ch} of down to 25 nm are realized on the GeOI substrate. Benefiting from the excellent gate control by the FD-UTB recessed channel and high quality contacts by the recessed S/D, record high drain current exceeding 1 A/mm is achieved. A simplified PO method is demonstrated, effectively reducing the interface trap density. The interface-related device behaviors are also studied by the TCAD simulation. Through a fundamental analysis on the correlations between the Fermi-level and the TNL at Ge's interface, initially n-type doped channels are preferred for both AM nMOSFETs and IM pMOSFETs on Ge, which have better tolerance to the nonideal interface between high-κ and Ge. The Ge nMOSFETs demonstrated in this paper have the performance approaching the state-of-the-art Ge pMOSFETs, revealing the promising future of ultimate CMOS applications built solely on Ge.

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