Single Pulse Charge Pumping Measurements on GaN MOS-HEMTs: Fast and Reliable Extraction of Interface Traps Density

Sami Alghamdi, Mengwei Si, Hagyoul Bae, Hong Zhou, and Peide D. Ye, *Fellow, IEEE*

***Abstract*— In this article, we report on the single pulse charge pumping (SPCP) measurements as a method to extract the interface trap density (N_{it}) on the GaN metal–oxide–semiconductor high-electron-mobility transistors (MOS–HEMTs). The electron capture and emission processes are monitored in the time domain and studied during the rising and falling edges of a gate voltage pulse. Two different gate stacks are studied by SPCP including epitaxial $Mg_{0.25}$ $Ca_{0.75}O$ (MgCaO) and amorphous Al_2O_3. The signature charge pumping (CP) current peaks are observed enabling a direct extraction of N_{it} as low as 1.4×10^{11} cm^{-2} with gate voltage sweeping from OFF-state to ON-state in the GaN MOS-HEMT with epitaxial MgCaO gate stack. A significant reduction of N_{it} by the MgCaO gate stack compared to Al_2O_3 only gate stack is also confirmed by the SPCP method. SPCP realizes a direct N_{it} measurement on GaN transistors and confirms the high quality interface between the single crystalline epitaxial MgCaO and GaN. It is verified as a fast and reliable interface characterization method on III–V HEMTs, gate-all-around nanowire transistors, and 2-D transistors, which do not exhibit body contacts as the conventional Si transistors needed for conventional CP measurements.**

***Index Terms*— Charge pumping (CP), GaN, interface trap density, metal–oxide–semiconductor high-electron-mobility transistors (MOS-HEMT), single pulse.**

I. Introduction

GaN has been a leading material in high-frequency and high-power electronic devices for its superior properties such as a wide energy bandgap, high saturation velocity, high electron mobility, and an ability to form 2-D electron gas (2-DEG) in AlGaN/GaN heterostructure in high-electron-mobility transistor (HEMT) [1]–[15]. It has been reported that an epitaxial single crystalline magnesium calcium oxide (MgCaO) insulator, which is lattice-matched to GaN and grown by atomic layer deposition (ALD), would achieve a very high quality interface and subsequently low interface trap density (D_{it} with a dimension of cm$^{-2} \cdot$ eV^{-1} or N_{it} with a dimension of cm^{-2}) on top of GaN heterostructures [16]–[18]. However, these low D_{it} were generally measured using capacitance–voltage (C–V) and conductance methods and mostly on bulk GaN metal–oxide–semiconductor (MOS) capacitors and not directly on the transistors because the conventional methods including the Terman, ac conductance, and charge pumping (CP) methods [19]–[22] require an adequate body contact. Capacitance- and conductance-based D_{it} extraction methods on scaled MOSFETs are also used but is considered to be less accurate than that on large-area MOS capacitors. The subthreshold method using the subthreshold swing (SS) is an estimation of average D_{it} in the subthreshold region and does not consider the depletion capacitance. The state-of-the-art GaN transistors have a 2-DEG on insulating substrate, similar to Si ultrathin-body devices with floating body channels. Thus, an interface trap density extraction method with a high accuracy and direct measurement on GaN HEMTs is highly demanded and this methodology can also be extended to other emerging device research such as gate-all-around nanowire transistors and ultrathin-body transistors based on 2-D materials, where the channels are floating [23].

The single pulse CP (SPCP) method provides real-time monitoring of the capture and emission process of electrons from the interface traps, enabling us to investigate the interaction between electrons and interface defects and consequently obtain an accurate extraction of the interface trap density [24]. In the SPCP measurements, the signature characteristic in the CP current peaks is used for the direct extraction of N_{it}. In this article, for the first time, we apply the SPCP approach to quantitatively study the N_{it} on GaN MOS-HEMTs. N_{it} is determined to be as low as 1.4×10^{11} cm^{-2} with gate voltage sweeping from OFF-state to ON-state in a GaN MOS-HEMT with epitaxial MgCaO gate stack. A significant N_{it} reduction is achieved compared to GaN MOS-HEMT with Al_2O_3 only gate stack, being consistent with our previous reports using MOS capacitors by the conductance method and UV-assisted C–V measurements [17], [18].

II. Experiment

Fig. 1(a) shows a cross-sectional schematic of an AlGaN/GaN MOS-HEMT with 4-nm MgCaO and 2-nm

Manuscript received August 21, 2019; revised October 24, 2019 and December 13, 2019; accepted December 17, 2019. Date of publication January 13, 2020; date of current version January 27, 2020. This work was supported by the Air Force Office of Scientific Research (AFOSR). The review of this article was arranged by Editor B. Kaczer. *(Corresponding author: Peide D. Ye.)*

Sami Alghamdi is with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA, with the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA, and also with the Department of Electrical and Computer Engineering, King Abdulaziz University, Jeddah 21589, Saudi Arabia.

Mengwei Si, Hagyoul Bae, Hong Zhou, and Peide D. Ye are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA, and also with the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2019.2961090

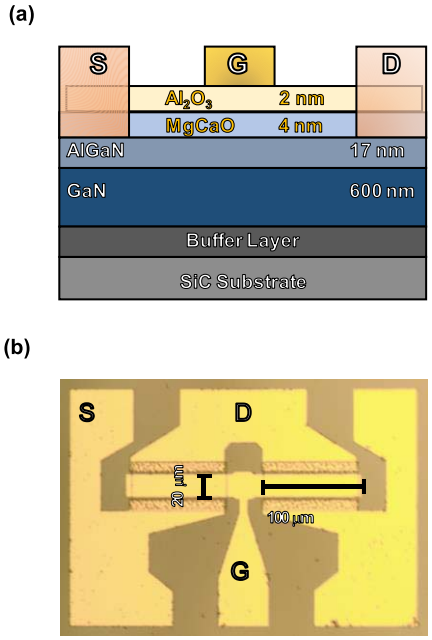

Fig. 1. (a) Schematic of an AlGaN/GaN MOS-HEMT with epitaxial MgCaO gate stack. (b) Microscope top-view image of fabricated devices, showing a channel length of 20 μm and channel width of 100 μm.

Al_2O_3 gate stack. Fig. 1(b) shows a microscopic image of two fabricated devices (GSG structure) with 20-μm channel length (L_{ch}) and 100-μm channel width (W_{ch}) each. The detailed fabrication process of the experimental devices is described in [16]. An important fact is that epitaxial MgCaO, grown by ALD, is lattice-matched on the GaN material system and offers an unprecedented high-quality interface for the device. Keysight B1500A Semiconductor Device Analyzer, Keysight B1530A waveform generator/fast measurements unit (WGFMU) along with remote-sense and switch unit (RSU), and high precision Agilent E4980A LCR meter were used for dc, SPCP, and C–V measurements, respectively, and all measurements are done at room temperature in a N_2 environment. Fast I–V measurements were carried out using the shortest cabling possible to minimize parasitic effects, and the floating system's time delay was found to be near 5 ns, less than the B1530A's minimum effective current sampling interval of 10 ns.

III. Results and Discussion

Fig. 2(a) shows the I_D–V_{GS} characteristics at a drain-to-source voltage (V_{DS}) of 0.1 V. A small hysteresis of 6.7 mV is extracted from Fig. 2(a) at 1 μA/mm, suggesting a high-quality interface. Fig. 2(b) shows the transconductance (g_m) characteristics. A threshold voltage (V_{th}) of −5 V is extracted by linear extrapolation method at low V_{DS}. Except for the negligible hysteresis in a transfer curve, the maximum g_m shows a slight difference. Note that the gate voltage at the maximum g_m point is not changing as shown in Fig. 2(b), indicating the threshold voltage difference between forward and reverse gate voltage sweeps is rather small, which is consistent with the extracted 6.7 mV hysteresis. Therefore, the difference in the g_m values is the result of carrier mobility difference between forward and reverse gate voltage sweeps.

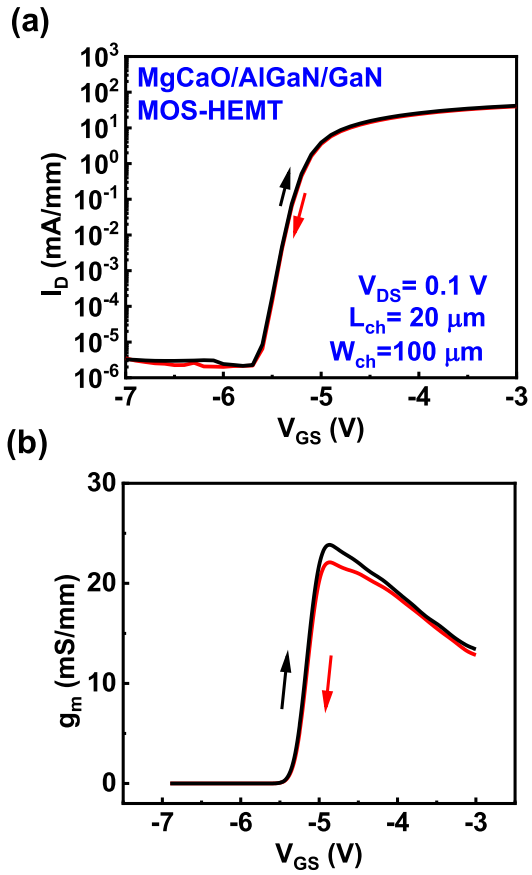

Fig. 2. (a) Transfer and (b) transconductance (g_m) characteristics of a representative AlGaN/GaN MOS-HEMT with epitaxial MgCaO gate stack, measured at V_{DS} = 0.1 V. The device has a channel length of 20 μm and channel width of 100 μm.

The mobility difference may be due to the different amounts of charge-induced mobility degradation.

In an SPCP measurement, a single voltage pulse is applied in the gate terminal (V_G), while the source and drain (S/D) are connected and grounded as the S/D terminal. The current flow from the gate terminal to S/D terminal is measured as the transient CP current (I_{tcp}). The electron transport processes in the SPCP measurement are illustrated in Fig. 3. SPCP measurement begins by an application of a sufficiently high gate voltage pulse at a sufficiently low base voltage (V_{BASE}) to switch the channel from depletion to accumulation. During the rising edge of the pulse, electrons from source and drain are pumped into the conduction band of the channel [from (a) initial state to (b) channel electron accumulation] and then captured by interface states [(c) electron capture], while channel electron depletion to source and drain takes place during the falling edge as described (d), where E_C is the conduction band, E_V is the valence band, and E_F is the Fermi level. The electron trapping process in the interface trap states is much slower than channel electron accumulation, where the mobile carriers come from source and drain. As a result, at the beginning of the falling edge, only the accumulating electrons in the conduction band are fast enough to go back to the source and drain. The current response difference between the rising edge and falling edge is the interface trap response, originated from the charge-trapping process. The electron emission from

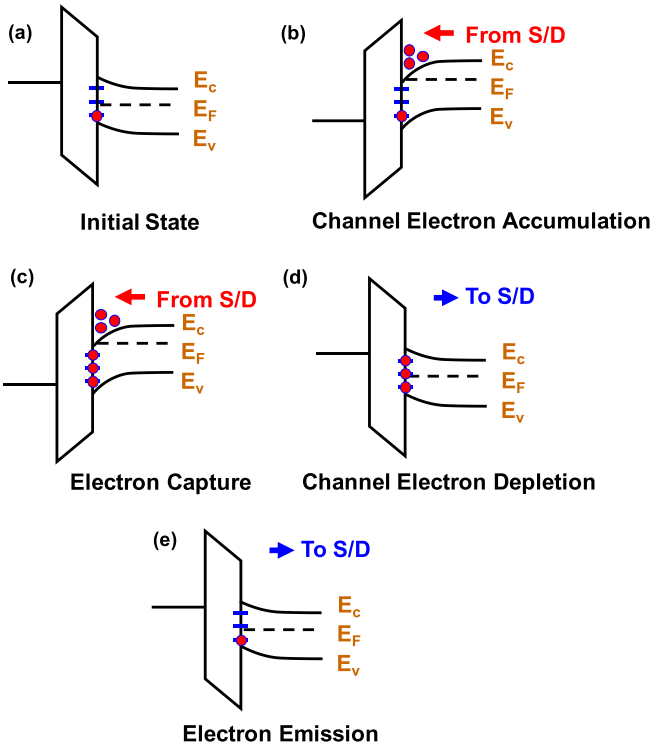

Fig. 3. Sequence of electron transport process in the rising and falling edges of the SPCP measurements, and the corresponding band diagrams: (a) initial state, (b) channel electron accumulation, (c) electron capture, (d) channel electron depletion, and (e) electron emission.

interface trap states as described in (e) is slow and leads to a broad tail at the end of transient CP current. Fig. 4 shows an example of SPCP measurement and the corresponding electron transport processes are highlighted. Note that deep traps with very long capture and emission time are not probed and not responsible for the transient CP current. The estimation of trap energy level by SPCP still needs further exploration. The accumulation electron charge is defined as Q_{acc} and the total charge of trapped electrons is defined as Q_{it}, where Q_{it} is qN_{it} and q is the elementary charge. Note that the CP current response is the superposition of traps responses from dielectric/AlGaN interface, AlGaN/GaN interface and also bulk traps in dielectric/AlGaN/GaN structure. Therefore, the N_{it} measured in this article is an effective 2-D trap density considering all these trap origins. In this article, the N_{it} extracted from GaN MOS-HEMT with the MgCaO gate stack is much smaller than the N_{it} extracted from GaN MOS-HEMT with Al_2O_3 only gate stack, indicating that the dielectric/AlGaN interface has an essential impact on the CP current response.

The rise time (t_{RISE}) and fall time (t_{FALL}) of the gate voltage pulse, as well as pulse width interval (t_{INT}) are varied, and the response of transient CP current, I_{tcp}, is then monitored. Sharp current peaks (as the trap response) during capture process and broad tails during emission were observed, as shown in Fig. 4. These two signature behaviors in I_{tcp} are attributed to the interface traps [23]–[29], which are utilized in SPCP to estimate the N_{it} of GaN MOS-HEMT.

The integration of the transient CP current during rise time ($I_{\text{tcp,RISE}}$) is the total charge including Q_{acc} and Q_{it}, as shown

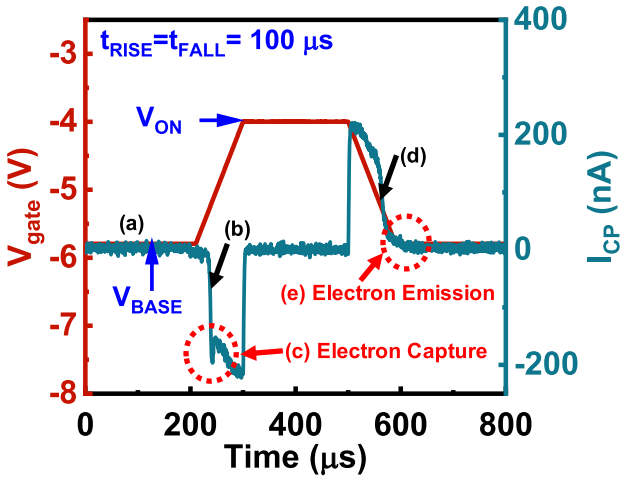

Fig. 4. Illustration of the applied gate pulse with the resulting transient CP current as a function of time. (a) Initial state, (b) channel electron accumulation, (c) electron capture, (d) channel electron depletion, and (e) electron emission.

in (1). The integration of the transient CP current during fall time ($I_{\text{tcp,FALL}}$) is the total charge of Q_{acc} only, as shown in (2)

$$Q_{\text{acc}} + Q_{\text{it}} = \int I_{\text{tcp,RISE}}\, dt \tag{1}$$

$$Q_{\text{acc}} = \int I_{\text{tcp,FALL}}\, dt. \tag{2}$$

Q_{it} can be calculated, according to (1) and (2), to subtract the impact of Q_{acc}. Equation (3) is then used to calculate the Q_{it}. In detail, Q_{it} is extracted by the curves of the two CP currents as follows: the rising edge current is flipped vertically, falling edge current is flipped horizontally, and then both are superimposed in order to determine charge difference as the interface charge Q_{it} from the area under the superimposed curves, as shown in Fig. 5(a). Note that in Fig. 5(a) inside the red square, the transient CP current in response to the rising edge ($I_{\text{tcp,RISE}}$) has a peak above the transient CP current in response to the falling edge ($I_{\text{tcp,FALL}}$) due to the electron capture in the trap state. The trap emission process is slow and behaves like a tail in the $I_{\text{tcp,FALL}}$ as shown by the blue square in Fig. 5(a). Therefore, to extract N_{it}, only the capture process is considered, as shown by the shaded area in Fig. 5(b)

$$Q_{\text{it}} = \int (I_{\text{tcp,RISE}} - I_{\text{tcp,FALL}})dt. \tag{3}$$

N_{it} is then estimated using $Q_{\text{it}} = qN_{\text{it}}$. Repeated measurements on the same device at different time periods are performed as shown in Fig. 5. The CP current responses almost overlap with each other at two subsequent measurements, as shown in Fig. 5(a). The extracted N_{it} value on these two measurements is very similar, as shown in Fig. 5(b). Therefore, the SPCP measurements are repeatable and reliable.

The electron capture and emission processes from interface states are examined with various characteristic ramping times (t_R) of the gate pulse where $t_R = t_{\text{RISE}} = t_{\text{FALL}}$. The measured interface trap density is similar using different t_{R} from 10 μs to 1 ms. In our measurements, t_{INT} is always chosen as $2t_R$ to ensure a full recovery between both edges. Fig. 6 shows the

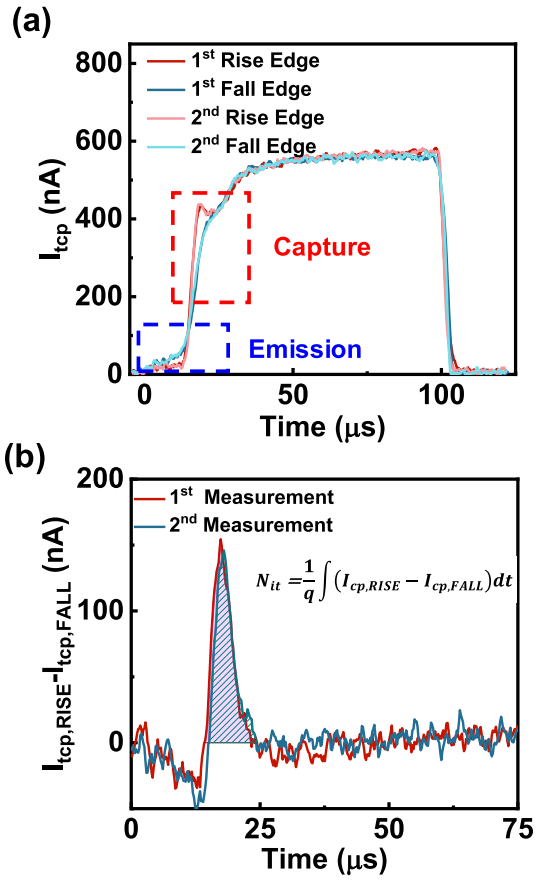

Fig. 5. (a) Comparison of CP current responses to rising edge and falling edge for multiple measurements. (b) Extraction of N_{it} by the integration of CP current difference between rising edge and falling edge.

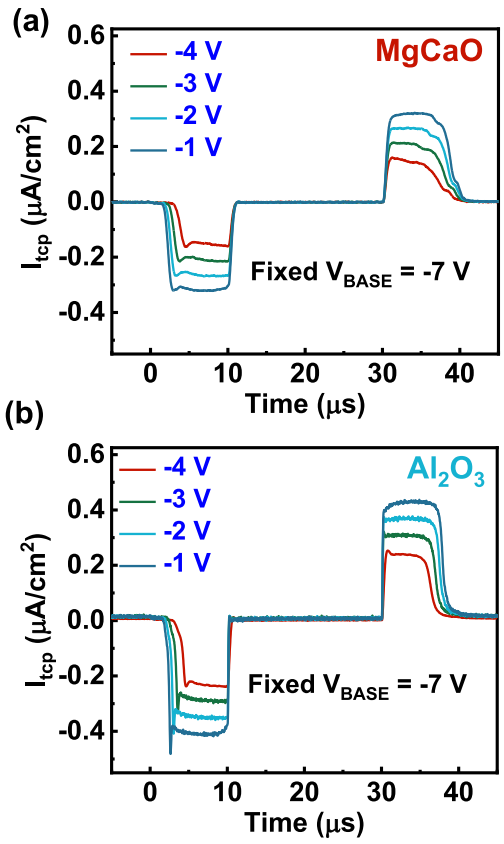

Fig. 6. Measured I_{tcp} versus time for multiple gate voltages V_{ON} for device with (a) epitaxial MgCaO gate stack and (b) Al_2O_3 only gate stack. Both rising and falling edges are shown as measured directly by SPCP. V_{BASE} is fixed at -7 V.

microscopic response of I_{tcp} with $V_{BASE} = -7$ V, multiple pulse voltages (V_{ON}) from -4 to -1 V, with $t_R = 10$ μs and $t_{INT} = 20$ μs, for both GaN-MOSHEMT with MgCaO gate stack and Al_2O_3 only gate stack. A sweeping gate voltage from depletion to accumulation and keeping V_{BASE} constant at -7 V (well below V_{th}) effectively changes the surface potential at the interface, thus, different trap energy levels (E_t) are accessed. SPCP measurements on GaN MOS-HEMTs with different gate dielectrics are studied and compared. Fig. 6(a) shows the SPCP measurements on GaN MOS-HEMT with epitaxial MgCaO gate stack, and Fig. 6(b) shows the SPCP measurements on GaN MOS-HEMT with Al_2O_3 only gate stack. A significant larger trap response (I_{tcp} peaks in response to rising edge of V_G) is observed on GaN MOS-HEMTs with Al_2O_3 only gate stack, suggesting a much lower interface trap density with epitaxial MgCaO/AlGaN interface.

Fig. 7 shows both $I_{tcp,RISE}$ and $I_{tcp,FALL}$ in the same timescale of the same measurement as in Fig. 6(a) for GaN MOS-HEMT with epitaxial MgCaO gate stack. The difference between $I_{tcp,RISE}$ and $I_{tcp,FALL}$ reflects the interface trap response as illustrated in Fig. 3(c) and (e). The N_{it} is evaluated according to (3) and the procedure shown in Fig. 5. Such N_{it} extraction is done on both GaN MOS-HEMT with MgCaO gate stack and Al_2O_3 only gate stack.

Fig. 8 shows a comparison of the extracted N_{it} as a function of V_{ON} with two different gate stacks: epitaxial

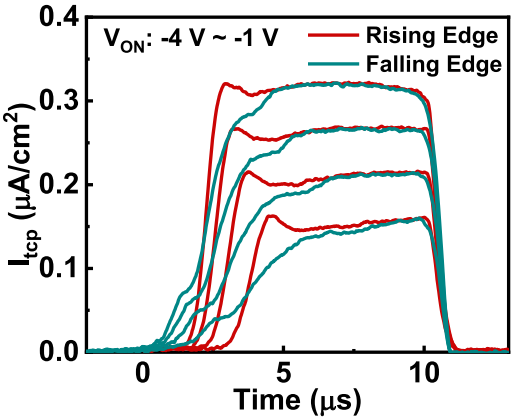

Fig. 7. Measured I_{tcp} in rising and falling edges as a function of time at different V_{ON}. V_{BASE} is fixed at -7 V. The current differences between rising edge and falling edge are compared for the purpose of N_{it} estimation.

MgCaO and Al_2O_3 only. The N_{it} in devices with MgCaO gate stack is found to be significantly smaller than the N_{it} in devices with Al_2O_3 only gate stack, suggesting a high quality MgCaO/AlGaN interface. This experimental data also indicate that the dielectric/AlGaN interface has a significant contribution to the overall trap response reflected in the CP current. Note that at ON-state the E_F change by V_{ON} is small, so that the extracted N_{it} does not have a significant change with respect to V_{ON}.

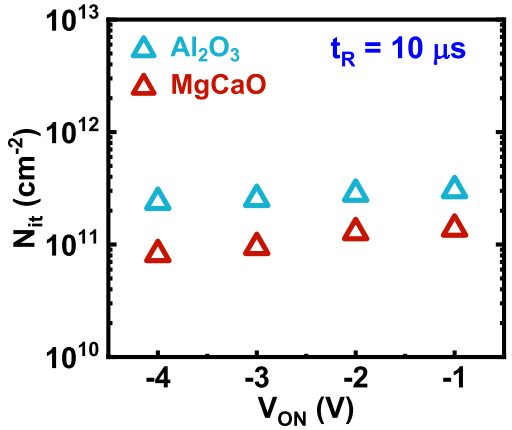

Fig. 8. Comparison of N_{it} versus V_{ON} using SPCP method on GaN MOS-HEMT with MgCaO gate stack and Al_2O_3 only gate stack.

IV. Conclusion

In summary, we report on the use of the SPCP measurements as a reliable method to directly monitor the capture and emission processes of the interface traps. As an accurate and fast technique to estimate N_{it} of the novel GaN MOS-HEMT, SPCP shows how electrons are captured by the interface states during the rising edge of the gate pulse and how it gets emitted in a slower way during the falling edge of the same pulse. N_{it} extracted via SPCP technique is significantly low down to 1.4×10^{11} cm^{-2}, suggesting a high-quality interface of epitaxial MgCaO on GaN devices. SPCP is verified as a promising technique for direct N_{it} estimation for state-of-the-art devices with floating body channels.

Acknowledgment

The authors would like to thank X. Lou, S. B. Kim, and R. G. Gordon from Harvard University on ALD of MgCaO.

References

[1] Y. Tang *et al.*, "Ultrahigh-speed GaN high-electron-mobility transistors with f_T/f_{max} of 454/444 GHz," *IEEE Electron Device Lett.*, vol. 36, no. 6, pp. 549–551, Jun. 2015, doi: 10.1109/led.2015.2421311.

[2] Y.-F. Wu *et al.*, "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 117–119, Mar. 2004, doi: 10.1109/led.2003.822667.

[3] K. Shinohara *et al.*, "Deeply-scaled self-aligned-gate GaN DH-HEMTs with ultrahigh cutoff frequency," in *Proc. Int. Electron Devices Meeting*, Dec. 2011, pp. 19.1.1–19.1.4, doi: 10.1109/iedm.2011.6131582.

[4] D. Xu *et al.*, "0.1-μm atomic layer deposition Al_2O_3 passivated InAlN/GaN high electron-mobility transistors for E-band power amplifiers," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 442–444, May 2015, doi: 10.1109/LED.2015.2409264.

[5] H. Sun *et al.*, "205-GHz (Al, In)N/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 957–959, Sep. 2010, doi: 10.1109/LED.2010.2055826.

[6] X. Zheng *et al.*, "N-polar GaN MIS-HEMTs on sapphire with high combination of power gain cutoff frequency and three-terminal breakdown voltage," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 77–80, Jan. 2016, doi: 10.1109/led.2015.2502253.

[7] K. D. Chabak *et al.*, "Strained AlInN/GaN HEMTs on SiC with 2.1-A/mm output current and 104-GHz cutoff frequency," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 561–563, Jun. 2010, doi: 10.1109/led.2010.2045099.

[8] K. D. Chabak *et al.*, "High-performance AlN/GaN HEMTs on sapphire substrate with an oxidized gate insulator," *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1677–1679, Dec. 2011, doi: 10.1109/led.2011.2167952.

[9] D. S. Lee *et al.*, "Impact of Al_2O_3 passivation thickness in highly scaled GaN HEMTs," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 976–978, Jul. 2012, doi: 10.1109/LED.2012.2194691.

[10] B. Song *et al.*, "Monolithically integrated E/D-mode InAlN HEMTs with f_t/f_{max} > 200/220 GHz," in *Proc. 70th Device Res. Conf.*, Jun. 2012, pp. 1–2, doi: 10.1109/DRC.2012.6257009.

[11] M. Higashiwaki, T. Mimura, and T. Matsui, "AlGaN/GaN heterostructure field–effect transistors on 4H-SiC substrates with current–gain cutoff frequency of 190 GHz," *Appl. Phys. Express*, vol. 1, Art. no. 021103, Feb. 2008, doi: 10.1143/apex.1.021103.

[12] A. L. Corrion *et al.*, "High-speed AlN/GaN MOS-HFETs with scaled ALD Al_2O_3 gate insulators," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1062–1064, Aug. 2011, doi: 10.1109/LED.2011.2155616.

[13] D. J. Meyer *et al.*, "High electron velocity submicrometer AlN/GaN MOS-HEMTs on freestanding GaN substrates," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 199–201, Feb. 2013, doi: 10.1109/LED.2012.2228463.

[14] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Influence of surface defect charge at AlGaN-GaN-HEMT upon Schottky gate leakage current and breakdown voltage," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 159–164, Feb. 2005, doi: 10.1109/ted.2004.842710.

[15] B. M. Green, K. K. Chu, E. Martin Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMT's," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 268–270, Jun. 2000, doi: 10.1109/55.843146.

[16] H. Zhou *et al.*, "DC and RF performance of AlGaN/GaN/SiC MOSHEMTs with deep sub-micron T-gates and atomic layer epitaxy MgCaO as gate dielectric," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1409–1412, Oct. 2017, doi: 10.1109/led.2017.2746338.

[17] H. Zhou *et al.*, "High-performance InAlN/GaN MOSHEMTs enabled by atomic layer epitaxy MgCaO as gate dielectric," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 556–559, May 2016, doi: 10.1109/led.2016.2537198.

[18] X. Lou *et al.*, "Epitaxial growth of $Mg_xCa_{1-x}O$ on GaN by atomic layer deposition," *Nano Lett.*, vol. 16, no. 12, pp. 7650–7654, Dec. 2016, doi: 10.1021/acs.nanolett.6b03638.

[19] K. Martens *et al.*, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 547–556, Feb. 2008, doi: 10.1109/ted.2007.912365.

[20] L. Terman, "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes," *Solid-State Electron.*, vol. 5, no. 5, pp. 285–299, Sep. 1962, doi: 10.1016/0038-1101(62)90111-9.

[21] G. Groeseneken, H. Maes, N. Beltran, and R. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. TED-31, no. 1, pp. 42–53, Jan. 1984, doi: 10.1109/t-ed.1984.21472.

[22] D. Cheney, R. Deist, J. Navales, B. Gila, F. Ren and S. Pearton, "Determination of the reliability of AlGaN/GaN HEMTs through trap detection using optical pumping," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp. (CSICS)*, Oct. 2012, doi: 10.1109/CSICS.2012.6340104.

[23] K. Taniguchi, N. Fang, and K. Nagashio, "Direct observation of electron capture and emission processes by the time domain charge pumping measurement of MoS_2 FET," *Appl. Phys. Lett.*, vol. 113, no. 13, Sep. 2018, Art. no. 133505, doi: 10.1063/1.5048099.

[24] L. Lin *et al.*, "A single pulse charge pumping technique for fast measurements of interface states," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1490–1498, May 2011, doi: 10.1109/ted.2011.2122263.

[25] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation-Model, monitor, and improvement," *IEEE J. Solid-State Circuits*, vol. 20, no. 1, pp. 295–305, 1985, doi: 10.1109/JSSC.1985.1052306.

[26] M. Hori, T. Watanabe, T. Tsuchiya, and Y. Ono, "Analysis of electron capture process in charge pumping sequence using time domain measurements," *Appl. Phys. Lett.*, vol. 105, no. 26, Dec. 2014, Art. no. 261602, doi: 10.1063/1.4905032.

[27] T. Watanabe, M. Hori, T. Tsuchiya, A. Fujiwara, and Y. Ono, "Time-domain charge pumping on silicon-on-insulator MOS devices," *Jpn. J. Appl. Phys.*, vol. 56, no. 1, Jan. 2017, Art. no. 011303, doi: 10.7567/jjap.56.011303.

[28] Z. Jian-Zhi *et al.*, "Determination of the relative permittivity of the AlGaN barrier layer in strained AlGaN/GaN heterostructures," *Chin. Phys. B*, vol. 18, no. 9, pp. 3980–3984, Sep. 2009, doi: 10.1088/1674-1056/18/9/060.

[29] J.-S. Lyu, "A new method for extracting interface trap density in short-channel MOSFETs from substrate-bias-dependent subthreshold slopes," *ETRI J.*, vol. 15, no. 2, pp. 10–25, Oct. 1993, doi: 10.4218/etrij.93.0193.0002.