Quantitative Characterization of Interface Traps in Ferroelectric/Dielectric Stack Using Conductance Method

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***Abstract*—In this work, the conductance method with an optimized circuit model is established to investigate the trapped charges at the ferroelectric/dielectric (FE/DE) interface. The density of interface states is quantitatively characterized to be $\sim 4 \times 10^{12}$ to 10^{13} $cm^{-2} \cdot eV^{-1}$. And the injection and accumulation of these enormous interfacial charges play a key role in the operation of the FE/DE stack. The proposed measurement technique provides a comprehensive understanding of the FE/DE stack as well as some new insights of negative capacitance effect and ferroelectric field-effect transistor device operations.**

***Index Terms*—Conductance method, ferroelectric/ dielectric (FE/DE), hafnium zirconium oxide, interface traps, leakage-assist-switching mechanism.**

I. Introduction

FERROELECTRIC-GATED field-effect transistor (FET) has been extensively studied for several years for its application on nonvolatile memory as ferroelectric FET (Fe-FET) [1]–[5]. The proposal of negative capacitance (NC) effect in ferroelectric devices exploits the development of NC-FET for low-power CMOS logic due to the steep subthreshold swing below 60 mV/decade [6]–[10]. No matter in Fe-FETs or NC-FETs, the ferroelectric/dielectric (FE/DE) stack is commonly applied, where the DE layer is inevitable in the form of native oxide or passivation layer for a substrate. Therefore, the study of the FE/DE stack is of great importance. It is well-known that the FE/DE stack is fundamentally different from an FE capacitor and a DE capacitor in series [12], [13]. It becomes complicated due to the FE/DE interfacial coupling effect and charge accumulation at the FE/DE interface [14]–[22]. It is a fact that there is a gap of charge mismatch between remnant polarization in FE layers and maximum tolerable charge density in DE layers [18]. The remnant polarization P_r of typical ferroelectric films is at the order of 10 $\mu C/cm^2$, whereas conventional dielectric insulators cannot support such a large charge density unless the existence of large leakage current and eventually the breakdown of dielectric. Thus, the leakage current and interfacial charges at the FE/DE interface are the only possible mechanism to make the polarization switching happen possible to satisfy the charge balance requirement [18]. In addition, the degradation of FeFETs has also been reported to be dominantly impacted by the interface properties, which is indicative of the significant FE/DE interfacial behavior during the operation of FE/DE stack [22]–[24]. However, the FE/DE interface trap properties have not been intensively and quantitatively investigated thoroughly.

Recently, a simultaneous I_d–V_g and polarization-voltage (P–V) measurements by the positive up negative down (PUND) pulse was applied to Fe-FETs to extract the defect density of interface [23]. By calculating the undesired non-ferroelectric hysteresis loop of I_d–V_g curves, a charge density of $\sim 10^{13}$ cm^{-2} at the FE/DE interface was obtained, which accounts for the stress-induced imprint voltage shift in the P–V loops. The charge density from this method is independent of polarization switching. Another novel split C–V technique combined with Hall measurement has been introduced to separate interface traps from the ferroelectric polarization charges in Fe-FETs, shown a surprisingly large trapped charge of $\sim 10^{14}$ cm^{-2} as the key role in the performance-boosting of transistors [20]. Nonetheless, the semiconductor/DE interface is also involved in the Fe-FETs, and the charge trapping at the semiconductor/DE interface might be confused with that at the FE/DE interface. To make the study of the FE/DE interface more distinct and straightforward, an FE/DE capacitor is more preferable.

In this work, the charge behaviors and interface trap properties at the FE/DE interface are quantitatively characterized in the structure of metal/FE/DE/metal capacitor. Hafnium

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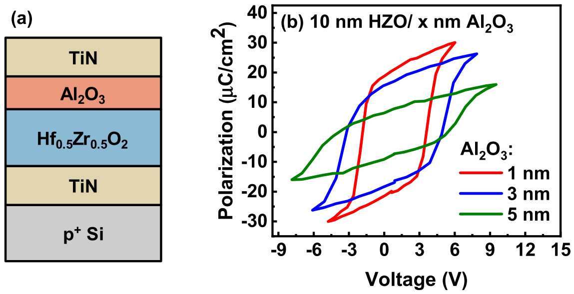

Fig. 1. (a) Cross section structure of the fabricated HZO/Al_2O_3 capacitor. (b) *P*–*V* hysteresis loops of the HZO/Al_2O_3 capacitors with 10-nm HZO and different Al_2O_3 thicknesses of 1, 3, and 5 nm.

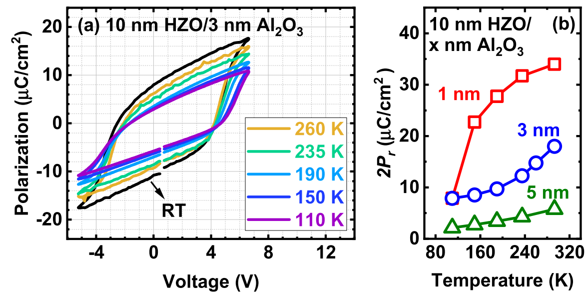

Fig. 2. (a) *P*–*V* hysteresis loops of the 10-nm HZO/3-nm Al_2O_3 capacitor at low temperatures from RT to 110 K. (b) Temperature dependence of P_r for the HZO/Al_2O_3 capacitor with different Al_2O_3 thicknesses.

zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$, HZO) is chosen as the FE layer and high-k insulator Al_2O_3 is chosen as the DE layer. P–V and C–V properties at different temperatures and frequencies are first measured to examine the existence of interface traps. Then, the conductance method, which is widely used for the study of the metal-oxide-semiconductor (MOS) interface [25], is formulated to measure the trap density at the FE/DE interface (D_{it}). Our previous work [21] reported the conductance peak phenomenon in FE/DE stack in C–V measurement. In this work, taking the consideration of leakage current through FE/DE stack and band bending fluctuation effect into the circuit and mathematical model for an accurate characterization of FE/DE interface trap behaviors are developed based on the main results of [21]. Using this optimized model, a distribution of D_{it} and the corresponding time constant τ_{it} at different polarization states are finally extracted at different temperatures. It is found that the charge trapping at the FE/DE interface, which is supplied from the leakage currents through the ultrathin DE layer, dominates the polarization switching of FE/DE stack.

II. Experiments

A. Capacitor Fabrication

Metal/FE/DE/metal capacitors were fabricated for the investigation of the FE/DE interface, as the cross-sectional schematic shown in Fig. 1(a). Heavily p-doped Si wafers with the resistivity less than 0.005 $\Omega \cdot$ cm were adopted as the substrate after standard solvent cleaning. As the metal contact, TiN was deposited by atomic layer deposition (ALD) at 250 °C, using the $[(CH_3)_2N]_4Ti$ and NH_3 as the Ti and N precursors, respectively. Alternating monolayers of HfO_2 and ZrO_2 were deposited by ALD at 200 °C to achieve an overall film composition of $Hf_{0.5}Zr_{0.5}O_2$ and a thickness of 10 nm, using $[(CH_3)_2N]_4Hf$, $[(CH_3)_2N]_4Zr$ and H_2O as the precursors of Hf, Zr, and O, respectively. To avoid cross-contamination, the TiN and HZO films were deposited in two separate chambers, which are connected externally by the Ar environment in a glove box to avoid environmental contamination. Next, the stacked Al_2O_3 layer with three different thicknesses (1, 3, 5 nm) was deposited by ALD at 200 °C, using $(CH_4)_3Al$ and H_2O as the Al and O precursors. Another TiN layer was deposited on the top of the HZO/Al_2O_3 stack. Both the bottom and top TiN films are metallic and have the same thickness of 30 nm. After deposition, all samples were annealed at 500 °C in the N_2 environment for 1 min by rapid thermal annealing to crystallize the HZO film. Then, Ti/Au top electrodes were fabricated by photolithography, e-beam evaporation, and a liftoff process. Dry etching was used to remove the top TiN layer by CF_4/Ar.

B. Electrical Characterization

Electrical characterizations at room temperature (RT) were probed in a Cascade summit probe station and low temperature experiments were conducted in a Lakeshore cryogenic probe station. The capacitance–voltage (C–V) and conductance measurements were taken using an Agilent E4980A impedance analyzer and P–V measurements were carried out using a Radiant RT66 ferroelectric tester. The applied voltage ranges were maximized in P–V measurements before the leakage current had essential impacts. All devices have already been woken up before the P–V characterization.

III. Results and Discussion

A. Temperature-Dependent P–V and C–V Properties

Fig. 1(b) shows the P–V curves of the HZO/Al_2O_3 capacitors with 10-nm HZO and different Al_2O_3 thicknesses from 1 to 5 nm. The ferroelectric hysteresis loops are observed which confirms the ferroelectricity of these HZO/Al_2O_3 capacitors. It is also found that the remnant polarization (P_r) decreases with the increasing Al_2O_3 thickness, which is due to the leakage-assist-switching mechanism [18]. The leakage currents through ultrathin Al_2O_3 layers with different thicknesses supply different quantities of mismatched charges for polarization switching, thus resulting in different P_r. These mismatched charges are essentially the trapped charges at the FE/DE interface.

To further demonstrate and investigate this charge trapping process, temperature-dependent P–V measurements were performed. Fig. 2(a) shows the P–V hysteresis loops for the 10-nm HZO/3-nm Al_2O_3 capacitor at low temperatures from 110 K to RT of 293 K. Temperature-dependent P_r is summarized in Fig. 2(b) for capacitors with different Al_2O_3 thickness. P_r decreases with the decreasing temperature, indicating the suppression of polarization switching. This phenomenon is the result of leakage current reduction through Al_2O_3 and the suppression of trap response at low temperatures, resulting in fewer trapped charges for polarization switching. It also indicates that the leakage-assist charge injection through the

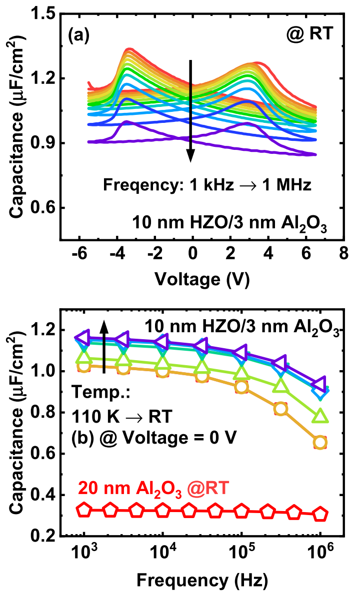

Fig. 3. (a) Frequency dispersion of $C-V$ properties for the 10-nm HZO/3-nm Al_2O_3 capacitor measured from 1 kHz to 1 MHz. (b) Frequency-dependent capacitance at zero bias voltage for the 10-nm HZO/3-nm Al_2O_3 capacitor measured from RT to 110 K. The capacitor with 20-nm Al_2O_3 in red is shown as the control sample.

FE/DE stack contains not only tunneling current but also thermionic emission process [26], [27]. Polarization switching at cryogenic temperatures suggests that both direct tunneling and trap-assisted tunneling are associated with the electron transport. Furthermore, P_r is found to decrease much more quickly in capacitors with thinner Al_2O_3, suggesting that thermionic emission contributes sufficiently to the leakage current transport.

$C-V$ characteristics were also measured at different frequencies and different temperatures. The frequency-dependent $C-V$ properties, ranging from 1 kHz to 1 MHz at RT, are shown in Fig. 3(a) for 10-nm HZO/3-nm Al_2O_3 capacitor. The capacitance decreases with the increasing frequency, as fewer traps respond to a higher frequency. The control sample, a capacitor with 20-nm Al_2O_3 dielectric layer only was also measured and its capacitance value keeps almost constant at the whole frequency regime, as the red symbols and line shown in Fig. 3(b). Therefore, this frequency dispersion is not induced by the measurement setup or parasitic effect. Fig. 3(b) shows the frequency-dependent capacitance value at low temperatures from RT down to 110 K. A smaller capacitance and larger frequency dispersion are observed at lower temperatures, which is attributed to the suppression of trap responses and charge injection. All these $P-V$ and $C-V$ measurement results under various temperatures and frequencies manifest the charge trapping at the FE/DE interface, supplied from leakage currents through the ultrathin DE layer, which is critical for the charge balance and polarization switching of FE HZO eventually.

B. Principle of Conductance Method for FE/DE Stack

The conductance method, proposed by Nicollian and Goetzberger [25], is a sensitive technique to determine the trap density at the MOS interface. As a loss mechanism,

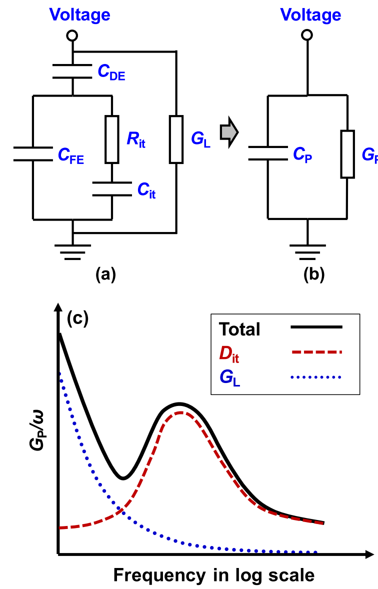

Fig. 4. (a) Equivalent circuit model for the conductance method applied to the FE/DE stack after considering the leakage current through the FE/DE stack. (b) Simplified equivalent circuit model for the conductance measurement by impedance analyzers. (c) Schematic of the G_P/ω and its components. The red dashed line and blue dotted line represent the interface trap-related D_{it} item and leakage current-related G_L term in (2), respectively. As a result, the black solid line shows an example of the conductance curve of FE/DE capacitors for the extraction of D_{it} and τ_{it}.

interface trap capture and emission of carriers are represented by the conductance. This trap resulted loss process, as well as capacitances in the MOS structure, are lumped to the parallel of an equivalent conductance and an equivalent capacitor. By applying a series of small-signal sine waves with different frequencies, this equivalent parallel conductance is measured, then the interface trap density and time constant can be obtained by fitting the measurement results to a theoretical circuit model. Comparing the possible equivalent circuit model of FE/DE stack with that MOS capacitor, the conductance method can also be applied to extract properties of the FE/DE interface traps.

Fig. 4(a) shows the proposed equivalent circuit of FE/DE stack, which is similar to that of MOS capacitors. The branch, including interface trap-related resistance R_{it} and capacitance C_{it}, is parallelly connected with the FE capacitance C_{FE} and then connected with the DE capacitance C_{DE} in series. Here, the interaction of interface traps with polarization charges by D_{it} ($C_{it} = qD_{it}$) is a lossy process, represented by R_{it}. A conductance component G_L is introduced because of the leakage currents through the FE/DE stack. It will not affect the measurement result of interface traps, which will be explained later.

Because the impedance analyzers generally assume the device under test to consist of the parallel of measured conductance G_P and measured capacitance C_P, one can replace the circuit of Fig. 4(a) by that in Fig. 4(b) for convenience, assuming negligible series resistance in the system. Thus, the total admittance Y_{it} of Fig. 4(a) can be normalized into the parallel connection of conductance G_P and capacitance C_P with

$$Y_{it} = G_P + j\omega C_P \tag{1}$$

and

$$\frac{G_P}{\omega} = \frac{(\omega\tau_{it})C_{DE}^2 C_{it}}{(\omega\tau_{it})^2(C_{FE}+C_{DE})^2+C_A^2} + \frac{G_L}{\omega} \tag{2}$$

$$C_P = \frac{C_A C_{FE}(C_{it}+C_{DE}) + (\omega\tau_{it})^2 C_{FE}C_{DE}(C_{FE}+C_{DE})}{(\omega\tau_{it})^2(C_{FE}+C_{DE})^2+C_A^2} \tag{3}$$

where ω is proportional to the measurement frequency f, and τ_{it} is equal to $R_{it}C_{it}$. Here, for a clear description, C_A is the sum of all capacitances, defined as

$$C_A = C_{FE} + C_{DE} + C_{it}. \tag{4}$$

To demonstrate the validity of this circuit model, the component of C_P is analyzed first. It can be expressed as (5) when extending ω to zero and as (6) when to infinity

$$C_P = \frac{C_{DE}(C_{FE}+C_{it})}{C_{FE}+C_{DE}+C_{it}}(\omega \to 0) \tag{5}$$

$$C_P = \frac{C_{DE}C_{FE}}{C_{FE}+C_{DE}}(\omega \to \infty). \tag{6}$$

It is found that C_P is the serial connection of C_{DE} and C_{FE} at high frequency. However, at low frequency, C_P includes an extra branch of C_{it} in parallel with C_{FE}. This changing tendency of C_P is consistent with the measurement result in Fig. 3(b), which can be theoretically explained by the frequency-related trap responses. The interface traps can respond to low-frequency signals but lag at high frequency. On the other hand, it is confirmed that for capacitors of 10-nm HZO/3-nm Al_2O_3, the numerical calculated C_P at RT, using (6) with the real C_{DE} (~1.9 $\mu F/cm^2$) and C_{FE}(~2.3 $\mu F/cm^2$), is approximate to the measured 0.95 $\mu F/cm^2$ as shown in Fig. 3(b). In addition, for all the measured devices with different Al_2O_3 thicknesses, the numerical calculated C_P using (6) with the real C_{DE} and C_{FE} have been confirmed to be approximate to the measured capacitance value at 1 MHz. Both phenomena indicate that the application of the conductance method with the optimized circuit model is valid to FE/DE capacitors.

As mentioned above, the relationship between G_P/ω and f can be utilized to quantitatively extract the properties of interface traps. Note that G_P in (2) is composed of two terms. For the first one, it is always equal to zero when assuming ω to be either zero or infinity, which means there must be a peak as the red dashed line shown in Fig. 4(c). As for the second term, G_L/ω is inversely proportional to f as the blue dotted line shown in Fig. 4(c). Here, this G_L can be obtained by measuring the leakage current of FE/DE capacitors. Although this term is important in low-frequency regimes, it can be negligible in high-frequency regimes where the peak appears. Note, this conductance of the leakage current of G_L from top to the bottom electrode does not contribute to a conductance peak. Consequently, by adding these two together, the final curve of G_P/ω versus f decreases first and then presents a peak with the generally increasing frequency, as the solid black line depicted in Fig. 4(c).

When carrying out the conductance measurement, a series of small ac signals with frequency changing over a wide range is applied to the FE/DE capacitors already biased at a constant voltage. Interfacial charges are resonances with the small ac signal at a certain frequency and then present a peak in the black solid line shown in Fig. 4(c). As (7) formulated, this peak value $(G_P/\omega)_{max}$ provides the information of D_{it} ($\underline{D}_{it} \equiv \underline{C_{it}/q}$) at the FE/DE interface. And τ_{it} can be obtained from the corresponding frequency ω_{peak} where the peak occurs using (8)

$$\left(\frac{G_P}{\omega}\right)_{max} = \frac{C_{DE}^2}{2(C_{FE}+C_{DE})C_A}C_{it} \tag{7}$$

$$\omega_{peak} = \frac{C_{FE}+C_{DE}+C_{it}}{(C_{FE}+C_{DE})\tau_{it}}. \tag{8}$$

However, a random distribution of discrete charges at the FE/DE interface makes the situation complicated and causes a deviation from the ideal case. With a nonuniform distribution of localized charges over the FE/DE interfacial plane, band bending fluctuation-induced τ_{it} dispersion should be considered. The Gaussian distribution is the most common statistical distribution characterized by only mean value and variance, which can be applied to describe this τ_{it} dispersion. Then, (2) for D_{it} extraction becomes

$$\frac{G_P}{\omega} = \int_{-\infty}^{+\infty} \frac{(\omega\tau_{it})C_{DE}^2 C_{it}}{(\omega\tau_{it})^2(C_{FE}+C_{DE})^2+C_A^2} P(\tau)d\tau + \frac{G_L}{\omega} \tag{9}$$

where $P(\tau)$ is a probability distribution of τ_{it} given by

$$P(\tau) = \frac{1}{\sqrt{2\pi\sigma_{it}^2}}\exp\left(-\frac{(\tau-\overline{\tau}_{it})^2}{2\sigma_{it}^2}\right) \tag{10}$$

where σ_{it} is the standard deviation of τ_{it} and $\overline{\tau}_{it}$ is the mean value of τ_{it}. Finally, D_{it} and τ_{it} at the FE/DE interface can be obtained by fitting the measured G_L, G_P, and C_P with the theoretical model given by (9) and (10).

It should be noted that the branch of R_{it} and C_{it} in Fig. 4(a) is connected to C_{FE} in parallel rather than C_{DE}, because this scheme has the best fit to experimental data (shown in Section III-C). This circuit scheme reveals that the FE/DE interface traps are most likely to be intrinsically related to the FE layer. Meanwhile, another four schemes were also attempted:1) connecting branch of R_{it} and C_{it} to C_{DE}; 2) only considering G_L through DE layer; 3) only considering G_L through FE layer; and 4) separating G_L into two components including one through DE layer and another through FE layer. By modeling and calculating, all these schemes were examined to be against the experimental observations, which cannot follow the trend of C_P and even contribute to a peak of G_P/ω.

C. Extraction of D_{it} and τ_{it}

Fig. 5(a) plots the measurement result of G_P/ω as a relationship to log frequency with negative bias voltages applied. And the results under positive bias voltage are shown in Fig. 5(b). Clear conductance peaks with different peak values are observed at different bias voltages, which can be used for the extraction of D_{it} and τ_{it}. And this conductance method has also been applied to the control samples, the metal/ferroelectric/metal capacitors with pure HZO film and metal/insulator/metal capacitors with pure Al_2O_3 film. There is no conductance peak observed in these two capacitors,

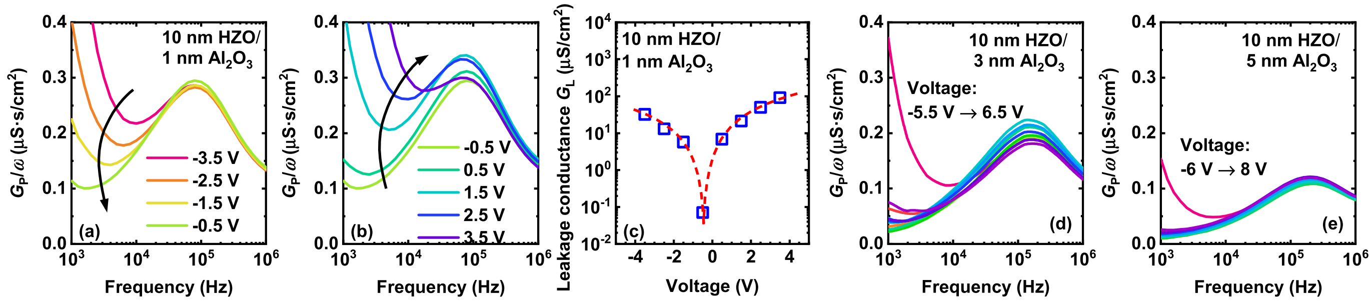

Fig. 5. Experimental results of the G_P/ω versus log f measured at different (a) negative and (b) positive bias voltages in the 10-nm HZO/1-nm Al_2O_3 capacitor. (c) Leakage conductance G_L of 10-nm HZO/1-nm Al_2O_3 under different bias voltages. (d) Experimental results of the G_P/ω versus log f at different voltages with 1 V/step, for the HZO/Al_2O_3 capacitors with the DE thickness of (d) 3 and (e) 5 nm.

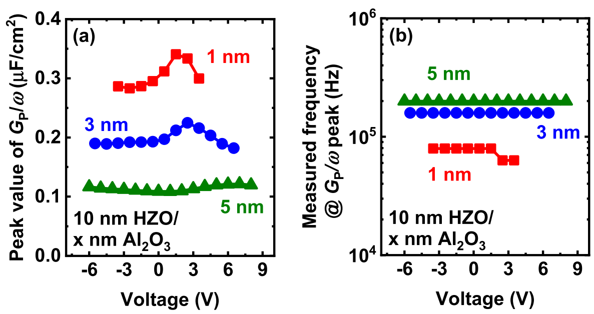

Fig. 6. Summarized (a) conductance peak values $(G_P/\omega)_{max}$ and (b) measured frequencies at peaks under different bias voltages for the HZO/Al_2O_3 capacitors with different thicknesses of Al_2O_3.

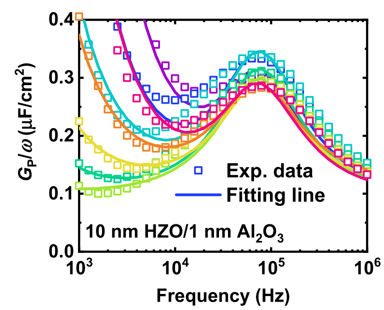

Fig. 7. Experimental data (squares) and fitting results (solid lines) of the conductance curve as a function of log frequency taken from the 10-nm HZO/1-nm Al_2O_3 capacitor. The bias voltage ranges from −3.5 to 3.5 V. Different color corresponds to that in Fig. 5.

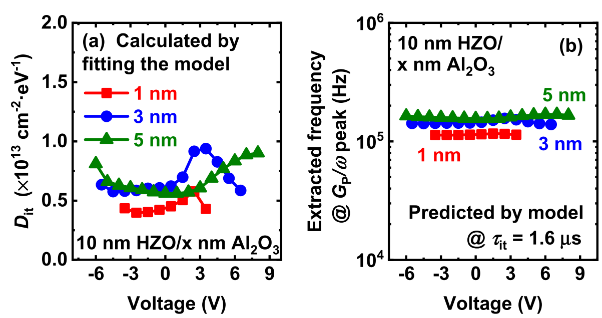

Fig. 8. (a) Calculated D_{it} of the HZO/Al_2O_3 capacitors with different Al_2O_3 thicknesses. (b) Peak frequency values predicted by the model when τ_{it} is around 1.6 μs.

illustrating the peak of G_P/ω in Fig. 5 is induced by the FE/DE interface rather than FE or DE layer itself. Besides, at low frequency of less than 10 kHz, the measured G_P/ω in Fig. 5(a) and (b) decreases as the absolute value of the negative bias voltage decreases. However, the measured G_P/ω increases with the increasing positive bias. This is due to the impact of G_L term in (9). The changing tendency of G_L is consistent with the measured I–V properties of this capacitor, as shown in Fig. 5(c). Through calculation, the peak value of G_P/ω has been verified to be hardly affected by this G_L term since the measured G_L is small and the ω_{peak} is large.

Furthermore, the measured G_P/ω as a function of log frequency is shown in Fig. 5(d) and (e) for the HZO/Al_2O_3 capacitors with 3- and 5-nm Al_2O_3, respectively. Fig. 6(a) and (b) summarizes these measured peak information of $(G_P/\omega)_{max}$ and ω_{peak} with an evolution of bias voltage, respectively. It is observed that $(G_P/\omega)_{max}$ decreases and ω_{peak} increases with the increasing Al_2O_3 thickness, suggesting different charge trapping behaviors. There are obvious peaks in the voltage distributions of $(G_P/\omega)_{max}$ appearing around coercive voltages while ω_{peak} almost keeps at the same value for a given DE thickness.

Fig. 7 gives an example of fitting results in the 10-nm HZO/1-nm Al_2O_3 capacitor by using the measured $(G_P/\omega)_{max}$ and G_L. The experimental data at different bias voltages exhibit good agreement with the theoretically fitting lines calculated by (9) and (10), which are favorable for the extraction of D_{it} and τ_{it}. This also verifies the validity of this technique for quantitative trap characterization at the FE/DE interface. Finally, the voltage distribution of D_{it} at different Al_2O_3 thicknesses are extracted and summarized in Fig. 8(a). It shows D_{it} is at the order of $\sim 4 \times 10^{12}$ to 10^{13} $cm^{-2} \cdot eV^{-1}$ and D_{it} increases obviously around coercive voltage, suggesting a strong charge trapping during polarization switching. The small discrepancy of D_{it} with different Al_2O_3 thicknesses illustrates that the thickness of the DE layer has little impact on the charge trapping, which demonstrates the assumption of intrinsic relationships between FE/DE interface traps and FE layer, mentioned in Section III-B.

It should be noted that this extracted D_{it} is the interface trap response to the small signals. It is fundamentally different from the charge density induced by ferroelectric polarization switching with large signal in [20] and [21]. The FE/DE capacitor has been biased at a constant voltage during the conductance measurement and the polarization switching has already finished. Moreover, the measured voltage distribution

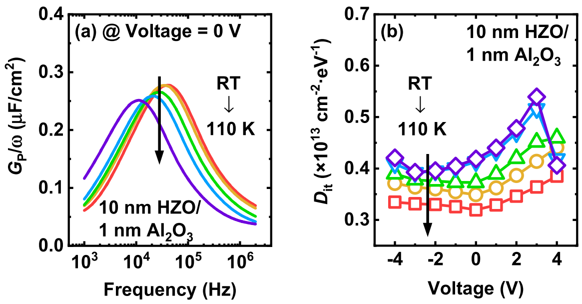

Fig. 9. (a) Measured G_P/ω with the relationship to frequency in log scale curves of the 10-nm HZO/1-nm Al_2O_3 capacitor at different temperatures ranging from RT to 110 K. (b) Extracted D_{it} distributions under different bias voltages at low temperatures.

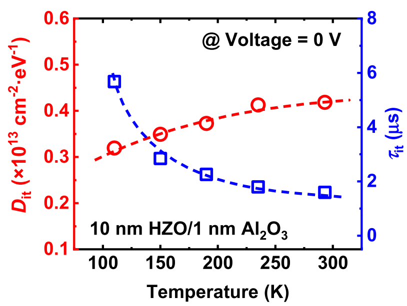

Fig. 10. Temperature-dependent D_{it} and τ_{it} at zero bias voltage ranging from RT to 110 K. Charge injection and trap response are suppressed at low temperatures.

of D_{it} corresponds to the trap density at different polarization states. By integrating them into the energy band during polarization switching, almost the same result with the data in [20] and [21] can be obtained. This accordance verifies that it is reasonable to adopt the conductance method to FE/DE stacks for D_{it} and τ_{it} extraction.

Fig. 8(b) shows the extracted ω_{peak} by the proposed model when assuming τ_{it} of $\sim$1.6 μs, which shows an approximative result with the measured in Fig. 6(b). Here, τ_{it} is assumed at the same value for FE/DE stacks with different Al_2O_3 thicknesses since R_{it} and C_{it} are mainly related to the FE layer in the equivalent circuit model for the conductance method, as shown in Fig. 4(a).

It also indicates that the charging/discharging process at the FE/DE interface could be effectively suppressed if the measurement frequency is up to more than 1 MHz, being consistent with the results in Fig. 3.

D. Behaviors of FE/DE Interface Traps at Low Temperature

To further understand the behaviors of FE/DE interface traps, the conductance method was also applied to 10-nm HZO/1-nm AlO_3 capacitors at low temperatures. Fig. 9(a) shows the experimental G_P/ω with a relationship to log frequency at zero bias voltage measured from RT to 110 K. Fig. 9(b) shows the extracted voltage-dependent D_{it} at different temperatures. The peak value and frequency at peak both decrease with the decreasing measurement temperature.

As summarized in Fig. 10, D_{it} at the FE/DE interface is smaller at lower temperatures, due to a weaker charge trapping/detrapping process, which suggests the reduction of leakage current through the DE layer and the suppression of trap response at the FE/DE interface. This phenomenon also agrees well with C–V measurement results in Fig. 3(b). In addition, τ_{it} was extracted and shown as the blue squares in Fig. 10. As the temperature decreases, a larger τ_{it} can be found. This can be attributed to the fact that charge injection is inhibited and trap response is slowed down.

IV. Conclusion

In conclusion, the FE/DE interface is experimentally investigated in a simple capacitor structure using the conductance method with an improved circuit model. The components and connection of the circuit model for the conductance method are analyzed in detail, and the nonuniform trap distribution is also taken into consideration. With the proposed measurement technique, the D_{it} at different static polarization states is obtained to be $\sim 4 \times 10^{12}$ to 10^{13} $cm^{-2} \cdot eV^{-1}$, indicating a critical role of charge trapping at the FE/DE interface during the operation of FE/DE stack. Besides, the smaller D_{it} and larger τ_{it} at low temperatures confirm the suppression of trap response. This conductance method provides a new approach and possible new insights to understand the mechanism of NC-FETs and Fe-FETs operations and their reliability degradations.

References

[1] J. Müller *et al.*, "Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 99, no. 11, 2011, Art. no. 112901, doi: 10.1063/1.3636417.

[2] T. P. Ma and J.-P. Han, "Why is nonvolatile ferroelectric memory field-effect transistor still elusive?" *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 386–388, Jul. 2002, doi: 10.1109/LED.2002.1015207.

[3] S. Müller *et al.*, "From MFM capacitors toward ferroelectric transistors: Endurance and disturb characteristics of HfO_2-based FeFET devices," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4199–4205, Dec. 2013, doi: 10.1109/TED.2013.2283465.

[4] H. Ishiwara, T. Shimamura, and E. Tokumitsu, "Proposal of a single-transistor-cell-type ferroelectric memory using an SOI structure and experimental study on the interference problem in the write operation," *Jpn. J. Appl. Phys.*, vol. 36, no. 3S, pp. 1655–1658, 1997, doi: 10.1143/JJAP.36.1655.

[5] M. Jerry *et al.*, "Ferroelectric FET analog synapse for acceleration of deep neural network training," in *IEDM Tech. Dig.*, Dec. 2017, pp. 139–142, doi: 10.1109/IEDM.2017.8268338.

[6] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, Feb. 2008, doi: 10.1021/nl071804g.

[7] K.-S. Li *et al.*, "Sub-60 mV-swing negative-capacitance FinFET without hysteresis," in *IEDM Tech. Dig.*, Dec. 2015, pp. 620–623, doi: 10.1109/IEDM.2015.7409760.

[8] M. H. Lee *et al.*, "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," in *IEDM Tech. Dig.*, Dec. 2016, pp. 306–309, doi: 10.1109/IEDM.2016.7838400.

[9] M. Si *et al.*, "Steep-slope hysteresis-free negative capacitance MoS_2 transistors," *Nature Nanotechnol.*, vol. 13, no. 1, pp. 24–28, Jan. 2018, doi: 10.1038/s41565-017-0010-1.

[10] W. Chung, M. Si, and P. D. Ye, "First demonstration of ge ferroelectric nanowire FET as synaptic device for online learning in neural network with high number of conductance state and Gmax/Gmin," in *IEDM Tech. Dig.*, Dec. 2018, pp. 344–347, doi: 10.1109/IEDM.2018.8614516.

[11] A. I. Khan, U. Radhakrishna, K. Chatterjee, S. Salahuddin, and D. A. Antoniadis, "Negative capacitance behavior in a leaky ferroelectric," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4416–4422, Nov. 2016, doi: 10.1109/TED.2016.2612656.

[12] Z. Liu, M. A. Bhuiyan, and T. P. Ma, "A critical examination of 'quasi-static negative capacitance' (QSNC) theory," in *IEDM Tech. Dig.*, Dec. 2018, p. 31, doi: 10.1109/.IEDM.2018.8614614.

[13] Y. J. Kim *et al.*, "Interfacial charge-induced polarization switching in Al_2O_3/Pb(zr,Ti)O_3 bi-layer," *J. Appl. Phys.*, vol. 118, no. 22, Dec. 2015, Art. no. 224105, doi: 10.1063/1.4937544.

[14] F.-C. Sun, M. T. Kesim, Y. Espinal, and S. P. Alpay, "Are ferroelectric multilayers capacitors in series?" *J. Mater. Sci.*, vol. 51, no. 1, pp. 499–505, Jan. 2016, doi: 10.1007/s10853-015-9298-0.

[15] Y. J. Kim *et al.*, "Time-dependent negative capacitance effects in Al_2O_3/$BaTiO_3$ bilayers," *Nano Lett.*, vol. 16, no. 7, pp. 4375–4381, Jul. 2016, doi: 10.1021/acs.nanolett.6b01480.

[16] M. Hoffmann, B. Max, T. Mittmann, U. Schroeder, S. Slesazeck, and T. Mikolajick, "Demonstration of high-speed hysteresis-free negative capacitance in ferroelectric $Hf_{0.5}Zr_{0.5}O_2$," in *IEDM Tech. Dig.*, Dec. 2018, pp. 727–730, doi: 10.1109/IEDM.2018.8614677.

[17] M. A. Alam, M. Si, and P. D. Ye, "A critical review of recent progress on negative capacitance field-effect transistors," *Appl. Phys. Lett.*, vol. 114, no. 9, Mar. 2019, Art. no. 090401, doi: 10.1063/1.5092684.

[18] M. Si, X. Lyu, and P. D. Ye, "Ferroelectric polarization switching of hafnium zirconium oxide in a ferroelectric/dielectric stack," *ACS Appl. Electron. Mater.*, vol. 1, no. 5, pp. 745–751, May 2019, doi: 10.1021/acsaelm.9b00092.

[19] K. D. Kim *et al.*, "Transient negative capacitance effect in atomic-layer-deposited Al_2O_3/$Hf_{0.3}Zr_{0.7}O_2$ bilayer thin film," *Adv. Funct. Mater.*, vol. 29, no. 17, Apr. 2019, Art. no. 1808228, doi: 10.1002/adfm.201808228.

[20] K. Toprasertpong, M. Takenaka, and S. Takagi, "Direct observation of interface charge behaviors in FeFET by quasi-static split C-V and Hall techniques: Revealing FeFET operation," in *IEDM Tech. Dig.*, Dec. 2019, pp. 570–573, doi: 10.1109/IEDM19573.2019.8993664.

[21] J. Li, Y. Qu, M. Si, X. Lyu, and P. D. Ye, "Multi-probe characterization of ferroelectric/dielectric interface by C-V, P-V and conductance methods," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 44–45.

[22] K. Ni *et al.*, "Critical role of interlayer in $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric FET nonvolatile memory performance," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2461–2469, Jun. 2018, doi: 10.1109/TED.2018.2829122.

[23] Y. Higashi *et al.*, "Impact of charge trapping on imprint and its recovery in HfO_2 based FeFET," in *IEDM Tech. Dig.*, Dec. 2019, pp. 358–361, doi: 10.1109/IEDM19573.2019.8993472.

[24] Y. Higashi *et al.*, "New insights into the imprint effect in FE-HfO_2 and its recovery," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar./Apr. 2019, pp. 1–7, doi: 10.1109/IRPS.2019.8720553.

[25] E. H. Nicollian and A. Goetzberger, "The si-sio, interface–electrical properties as determined by the metal-insulator-silicon conductance technique," *Bell Syst. Tech. J.*, vol. 46, no. 6, pp. 1033–1055, Jul./Aug. 1967, doi: 10.1002/j.1538-7305.1967.tb01727.x.

[26] V. Garcia and M. Bibes, "Ferroelectric tunnel junctions for information storage and processing," *Nature Commun.*, vol. 5, no. 1, pp. 1–12, Sep. 2014, doi: 10.1038/ncomms5289.

[27] M. Houssa *et al.*, "Trap-assisted tunneling in high permittivity gate dielectric stacks," *J. Appl. Phys.*, vol. 87, no. 12, pp. 8615–8620, Jun. 2000, doi: 10.1063/1.373587.