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Steep-slope hysteresis-free negative capacitance MoS₂ transistors

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Supplementary Information for:

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1. Fast I-V measurement of ferroelectric MOS capacitors



Figure S1 | **Illustration of MOS structure for Pulsed I-V measurement. a** Schematic diagram of a ferroelectric MOS capacitor for fast I-V measurement. **b** Optical image of the ferroelectric MOS capacitors from top view.

To study ferroelectric characteristics of the gate stack, a ferroelectric test structure is designed for fast I-V and C-V measurement. Fig. S1a shows the schematic of the ferroelectric MOS capacitor for test structure and Fig. S1b shows an optical image of the ferroelectric MOS capacitors. Hafnium zirconium oxide (HZO) was deposited by atomic layer deposition (ALD) for 20 nm as ferroelectric insulator layer on heavily doped silicon substrates. Another 10 nm aluminum oxide (Al₂O₃) layer was deposited as an encapsulation layer for capacitance matching and to prevent degradation of HZO due to air exposure. The annealing process was performed in rapid thermal annealing (RTA) in nitrogen ambient for 1 minute at various temperatures. Ti/Au with 30 nm/60 nm was used as electrode metal.

To validate the ferroelectricity of the gate stack used in this work, current response to a triangular voltage signal was measured to characterize the hysteresis loop of polarization versus electric field (P-E). All current responses from no RTA to 600 °C RTA deviate from a square wave signal, indicating the MOS capacitors measured in this work is not linear capacitors (Fig. S2a). The hysteresis loops of P-E at different temperatures are obtained from the integration of current response as a function of voltage, to obtain the polarized charge density¹. From the hysteresis loop of P-E, it is confirmed that the samples with 400 °C and 500 °C exhibit stronger ferroelectricity, compared to those with no RTA or 600 °C.

Grazing incidence X-ray diffraction (GI-XRD) analysis in Fig. S2d depicts the crystallization behaviors of HZO with no RTA and 400 °C. The sample with 400 °C reveals apparent orthorhombic phases (o-phases). The formation of non-centrosymmetric o-phase is believed to lead to the ferroelectricity of HZO films after annealing^{2,3}, as confirmed in Fig. S2b. The slightly crystallized HZO found in the sample with no RTA is attributed to the thermal budget of ALD Al₂O₃ deposition.



Figure S2 | **Ferroelectricity in the gate stack. a** Current response to a triangular voltage signal of the ferroelectric capacitor in Fig. S1 without RTA and with RTA from 400 °C to 600 °C in N₂ ambient for 1 min. **b** Temperature dependence of the P-E hysteresis curves obtained from a. **c** Current response of a linear capacitor with 20 nm Al_2O_3 only as dielectric. **d** GI-XRD diffractograms of HZO. The formation of non-centrosymmetric o-phase is believed to lead to the ferroelectricity of HZO films after annealing at 400°C.

2. Gate leakage current of MoS₂ NC-FETs



Figure S3 | Gate leakage current in MoS₂ NC-FETs. Gate leakage current and I_D -V_{GS} characteristics simultaneously measured in the MoS₂ NC-FET for Fig. 2c.

The gate leakage current was measurement simultaneously with I_D , as shown in Fig. S3. It is the gate leakage current and I_D -V_{GS} characteristics simultaneously measured in the MoS₂ NC-FET for Fig. 2c. A constant gate leakage current ~pA level means the gate leakage current is negligible in subthreshold region and the measured leakage is the lower detection limit of the equipment, as a medium power SMU is used for gate leakage current to speed up measurement here instead of a high-resolution SMU for I_D .

3. Effect of RTA temperature on the subthreshold slope of MoS₂ NC-FETs



Figure S4 | Statistic study of the effect of RTA temperature on the subthreshold slope and hysteresis of MoS₂ NC-FETs. a SS_{For}, b SS_{Rev,min#1}, c SS_{Rev,min#1}. d hysteresis. Each data point contains the measurement of at least 8 individual devices with the same fabrication process. The SS and hysteresis presented here are all from I_D -V_{GS} characteristics measured at 5 mV V_{GS} step. The hysteresis is measured as V_{GS}-difference between forward and reverse sweeps at I_D =1 nA/µm and at V_{DS}=0.1 V. All the devices have the device structure as shown in Fig. 1.

As the annealing temperature is quite critical to ferroelectricity of the gate stack, we carried out the statistic study of the effect of RTA temperature on the SS of $MoS_2 NC$ -FETs. As the RTA was performed after the gate stack deposition and before the transfer of MoS_2 flake, only the substrate, HZO and Al₂O₃ were affected. Fig. S4a-c shows the SS_{For}, SS_{Rev,min#1} and SS_{Rev,min#2} versus RTA temperature, respectively. It is found that devices with 400 °C RTA show the lowest SS for all three SS characteristics. Meanwhile, devices with 500 °C RTA have lower SS_{For} and SS_{Rev,min#1} than devices without RTA and devices with 600 °C RTA. This RTA temperature dependence of SS is very consistent with the results from Fig. S2. Devices with 400 °C or 500 °C RTA have lower SS comparing with devices without RTA or with 600 °C RTA because the stronger ferroelectricity, as shown in Fig. S2b. A statistic study on temperature dependent hysteresis is shown in Fig. S4d. It is found that MoS₂ NC-FETs with 500 °C RTA exhibit the lowest hysteresis comparing with devices without RTA, devices with RTA at 400 °C and 600 °C. All hysteresis data collected here is from I_D-V_{GS} characteristics measured in fast sweep mode with 5 mV V_{GS} step and at V_{DS}=0.1 V.

4. Layer number determination of MoS₂ flake and mono-layer MoS₂ NC-FET

Monolayer, bi-layer and multi-layer MoS₂ flakes were identified using three techniques: Raman shift⁴, photoluminescence spectra⁵ and AFM measurement⁶. There are two characteristic Raman modes, the in-plane vibrational mode and the out-of-plane vibrational mode with $\Delta \omega$ =18.5 cm⁻¹ indicating mono-layer and $\Delta \omega$ =21.4 cm⁻¹ indicating bi-layer, as shown in Fig. S5a. Meanwhile, mono-layer MoS₂ is well known to have a direct bandgap so that there is a strong peak in photoluminescence spectra as shown in Fig. S5b. It is straight forward to distinguish mono-layer MoS₂ from bi-layer or few-layer MoS₂. AFM measurement is also applied to determine the thickness and a mono-layer MoS₂ flake in this work is measured to be around 0.9 nm, as shown in Fig. S5c. Fig. S5d shows the I_D-V_{GS} characteristics of a mono-layer MoS₂ NC-FET. Severe SS degradation is observed at low V_{DS} due to the large Schottky barrier height for mono-layer MoS₂ at metal/channel contacts.



Figure S5 | **Mono-layer identification and monolayer MoS**₂ **NC-FET. a** Raman spectrum measurement of monolayer and bi-layer MoS₂. **b** Photoluminescence measurement of single-layer and bi-layer MoS₂. **c** AFM measurement of a mono-layer MoS₂ flake. **d** I_D-V_{GS} characteristics of a mono-layer MoS₂ NC-FET with 0.5 μm channel length.

5. Low temperature measurement of a bi-layer MoS₂ NC-FET

Fig. S6 shows the low temperature measurement of a bi-layer $MoS_2 NC$ -FET from 160 K to 220 K. The device has a channel length of 0.5 μ m and a channel width of 2.5 μ m. The low temperature electrical data was collected with a Lakeshore TTP4 probe station. Measured SS is below the thermionic limit down to 220 K. SS below 190 K shows above the thermionic limit because of stronger impact of Schottky barrier on SS.



Figure S6 | Low temperature measurement of a bi-layer MoS₂ NC-FET. I_D -V_{GS} characteristics of a bi-layer MoS₂ NC-FET with 0.5 μ m channel length, 2.5 μ m channel width. **a** 160 K. **b** 190 K. **c** 220 K. **d** 250 K. **e** 280 K.

6. Experiment setup for thermoreflectance imaging



Figure S7 | Illustration of thermoreflectance imaging measurement system. a A schematic of thermoreflectance imaging system. A pulse generator (V_{DS}) and a constant voltage source (V_{GS}) drive the transistor. A control computer triggers the illumination driver and the CCD camera for a given delay time with respect to V_{DS} . b Timing diagram for transient TR imaging with a given LED delay time (t_d).

The thermoreflectance (TR) measurement system setup is shown in Fig. S7^{7,8}. A highspeed LED pulse illuminates the device, and a synchronized chare coupled device (CCD) camera captures the reflected image, as shown in Fig. 7a. The MoS₂ is illuminated through an LED (λ = 530 nm) via an objective lens. The reflected light from the surface of MoS₂ channel is captured on a variable frame rate, 14-bit digitization, Andor CCD camera.

For the transient measurement of temperature, the device is periodically turned ON and OFF by a V_{DS} pulse, as shown in Fig. S7b, allowing the channel to heat and cool, respectively. By controlling the delay of the LED pulse with respect to the beginning of the V_{DS} pulse, the TR image can capture different phases of the transient heating and cooling kinetics. The delay time for the LED illumination can be varied and each illumination pulse acts as a camera shutter. Every V_{DS} cycle produces an image capturing the thermal state of the substrate at a given time delay. The

average of these images improves the signal-to-noise ratio and produces a high-resolution map of temperature. In this work, temperature was measured at the last 100 μ s of the 1 ms drain voltage pulse (10 ms period).

The change in reflectivity (ΔR) under visible spectral range is proportional to the change in temperature, so that once the TR coefficient is obtained, ΔR can be mapped to differential increase in temperature (ΔT_S). Unfortunately, TR coefficient must be calibrated, because it depends on the wavelength, the angle of incidence, and the polarization of the incident light, as well as the surface properties of the reflecting material. The calibration is performed by heating the sample by placing it on an external microthermoelectric stage. The temperature of the sample is monitored by micro-thermocouple while capturing the reflection changes by the CCD camera. The TR coefficient for the specific setup is obtained by plotting the change in reflectivity as a function of temperature measured by the thermocouple. Here, TR coefficient is calibrated on exfoliated MoS₂ flakes.

7. Simulation of MoS₂ NC-FETs

As shown in Fig. S8a a negative capacitance MoS_2 transistor can be treated as an intrinsic MoS_2 transistor in series with an HZO ferroelectric capacitor. In addition, the electrical behavior of HZO ferroelectric capacitor can be described by Landau-Khalatnikov (LK) equation⁹⁻¹¹. Landau coefficients are extracted from the experimental P-E curve of HZO. For the intrinsic MoS_2 transistor, one can obtain its transfer characteristic and output characteristic using classical drift-diffusion method. To simulate the experimental device (metal (Heavily-doped silicon)-ferroelectric oxide-insulator-semiconductor), we will assume that the potential distribution is essentially uniform across the gate dielectric, which simplifies the overall analysis by allowing one to decouple the HZO dielectric from the standard MOSFET structure¹²⁻¹⁴. In fact, the errors caused by this approximation can be ignored when the thickness of ferroelectric layer is not too thick^{15,16}. The other device parameters are extracted from the experimental transfer characteristics. All simulations assume 1 μ m channel length, 8.6 nm thick MoS₂ flake, and 2 nm Al₂O₃ capping, unless otherwise specified.

Landau coefficients (α , β , γ) are extracted from the P-E measurement on the TiN/HZO/TiN structure, as shown in Fig. S8c, in which ALD HZO process condition is exactly same as the one for the HZO/Al₂O₃ stacks but with TiN as top and bottom metallic electrodes. The complete LK equation is written as¹⁷,

$$V_{GS} = V_{mos} + V_f = V_{mos} + 2t_f \alpha Q_{av} + 4t_f \beta Q_{av}^3 + 6t_f \gamma Q_{av}^5 + \rho t_f \frac{dQ_{av}}{dt}$$
(1)

$$Q_{av} = \frac{Q_{ch} + Q_{p1} + Q_{p2}}{WL}$$
(2)

$$Q_{p1} = C_{fr} W_{ch} (V_{mos} - V_S) \tag{3}$$

$$Q_{p2} = C_{fr} W_{ch} (V_{mos} - V_D) \tag{4}$$

where Q_{av} is the average gate charges density per area. Q_{ch} is the intrinsic channel area charge, Q_{p1} is the parasitic charges caused by the source-gate capacitance, and Q_{p2} is the parasitic charges caused by the drain-gate capacitance. α , β , and γ are Landau coefficients, which are material dependent constants; t_f is the thickness of the ferroelectric film; and V_f is the external applied voltage across the ferroelectric layer. ρ is an equivalent damping constant of HZO.

The Landau coefficients are extracted to be α =-1.1911e8 m/F, β =4.32e9 m⁵/F/coul², and γ =0 m⁹/F/coul⁴, as shown in Fig. S8c. Fig. S8d shows the simulation results based on these experimental Landau coefficients which exactly match with our experimental results. Based on the Landau coefficients extracted from experimental P-E and eqn. (1), the capacitance of ferroelectric capacitor (C_{FE}) can be calculated using experimental Landau coefficients,

$$C_{FE} = \frac{dQ_{av}}{dV_f} = \frac{1}{2\alpha t_f + 12\beta t_f Q_{av}^2 + 30\gamma t_f Q_{av}^4}$$
(5)

The internal gain condition and the non-hysteretic condition for MoS₂ NC-FETs are discussed based on the experimental P-E and extracted Landau coefficients. To prevent hysteretic behavior and obtain a steep SS at the same time, some design rules must be obeyed. These design principles could be derived from its small-signal capacitance circuit of a 2D NC-FET as shown in Fig. S8b. SS can be written as,

$$SS = \frac{2.3k_BT}{q} \cdot \frac{1}{\frac{\partial \phi_S}{\partial v_{gs}}} = \frac{2.3k_BT}{q} \left(1 + \frac{c_{2D}}{c_{ox}} \right) \cdot \left(1 - \frac{c_{device}}{|c_{FE}|} \right)$$
(6)

$$C_{device} = 2C_{fr} + \frac{c_{2D}c_{ox}}{c_{2D} + c_{ox}}$$
(7)

Note that C_{fr} is the parasitic capacitance. SS must satisfy the condition, $0 < SS < 2.3k_BT/q$, so that non-hysteretic behavior and a sub-thermionic SS (internal gain>1) could be obtained at the same time. The constraint conditions as the equations (8, 9) deduced from (6) are,

$$C_{device} < |C_{FE}| \tag{8}$$

$$|\mathcal{C}_{FE}| < \mathcal{C}_{eq} \tag{9}$$

$$C_{eq} = \left(1 + \frac{c_{ox}}{c_{2D}}\right) \cdot C_{device} \tag{10}$$

If no parasitic capacitance is considered as C_{fr}=0, the constraint conditions and SS become,

$$\frac{c_{2D}c_{ox}}{c_{2D}+c_{ox}} < |C_{FE}|$$
(11)

$$|C_{FE}| < C_{ox} \tag{12}$$

$$SS = \frac{2.3k_BT}{q} \left(1 + \frac{C_{2D}(|C_{FE}| - C_{ox})}{|C_{FE}|C_{ox}}\right)$$
(13)

To satisfy non-hysteretic conditions, $|C_{FE}|$ need to be greater than C_{device} (eqn. (8)), while to satisfy internal gain condition (internal gain>1, SS<2.3k_BT/q), $|C_{FE}|$ need to be less than C_{eq} (eqn. (9)). Note that C_{eq} equals to C_{ox} if $C_{fr}=0$. C^{-1} of $|C_{FE}|$, C_{device} , and C_{eq} are compared as shown in Fig. S8e with different t_f . It is clear to see that if t_f is greater than 72.5 nm, $|C_{FE}|$ becomes smaller than C_{device} which is against eqn. (8) so that hysteresis will be introduced, as shown in Fig. S8f. If $|C_{FE}|$ is less than C_{eq} , the design satisfies the internal gain condition where SS can be less than 2.3 k_BT/q , as shown in Fig. S8e. When the gate voltage is in subthreshold region, $|C_{FE}|$ is less than C_{eq} among all t_f .

The internal gain condition and non-hysteresis condition are directly related with the C_{fr}. If C_{fr}=0, the internal gain condition ($|C_{FE}|<C_{ox}$) as eqn. (12), can't be fulfilled since the minimum $|C_{FE}|$ obtained for 20 nm HZO from eqn. (2) is about $|C_{FE}|=13.1 \ \mu\text{F/cm}^2$, which is larger than the C_{ox}=3.54 $\mu\text{F/cm}^2$ (2 nm Al₂O₃). Therefore, C_{fr} must be considered to fulfill the internal gain conditions, as calculated in Fig. S8e. With the existence of C_{fr}, $|C_{FE}|$ can be smaller than C_{eq}, which fulfills the internal gain condition in eqn. (9). Fig. S8g shows the impact of C_{fr} on the SS vs. I_D characteristics. It is clear that if C_{fr}=0, the SS of the MoS₂ NC-FET is the same as 2.3k_BT/q so that no internal gain can be obtained as predicted by eqns. (12, 13). However, if we consider the impact

of C_{fr} , SS can be less than 2.3 k_BT/q (internal gain>1) because eqn. (9) is fulfilled as shown in Fig. 8e.

Fig. 8h shows the t_{ox} - t_f design plane of the device. The boundary line between two regions represents the capacitance match: - $C_{FE}=C_{device}$. The cyan area represents the design space of transfer characteristics with non-hysteresis and a steep SS. Even though the subthreshold slope would be reduced when t_f increases, the hysteresis must be avoided in logic applications. Thus, the device geometries (t_f - t_{ox}) should be co-optimized to avoid the hysteresis and achieve a steep SS at the same time.

The simulation results MoS₂ NC-FETs are discussed in details after satisfying the internal gain and non-hysteretic conditions. As shown in Fig. S9a, it can be observed that IDS decreases obviously as t_f increases for a given gate voltage when the device works in the depleted regime (V_{GS}<V_{FB}). V_{FB} is defined as the gate voltage when the total gate (or channel) charges reaches zero. In a junctionless transistor, this critical voltage differentiates between depletion-mode subthreshold operation vs. accumulation mode above threshold operation¹⁵. Note that V_{FB} is bigger than V_{FB0} (flat-band voltage when V_{DS}=0 V) because there is a depleted region in the drain terminal when V_{DS} is not zero. Thus, the increasing of t_f lowers the off-state current significantly and improve threshold voltage compared with its conventional MoS₂ transistor (when t_f=0 nm, a MoS₂ NC-FET is reduced to a MoS₂ transistor). In contrast, in the on-state accumulation regime (V_{GS}>V_{FB}), I_{DS} increases when t_f increases. In other words, both on and off state performances improve with t_f, so long the transistor is operated in the NC-FET mode. The phenomenon can be explained as follows. Fig. S9b shows that the interfacial potential (V_{mos}) varying with V_{GS} for different tf. When VGS is smaller than VFB (in the depleted regime), Vmos deceases with tf increasing while when V_{GS} is bigger than V_{FB} (in the accumulation regime), V_{mos} increase with t_f increasing.

Thus, the off-state current can be lowered and on-state current can be improved at the same time. Among the range of HZO thicknesses possible, $t_f=20$ nm was chosen for processing convenience.

For drift-diffusion based transistors, the subthreshold slope can be estimated as 2.3 $k_BT/(d\varphi_S/dV_{GS})$. For negative capacitance FETs, the DC voltage gain (defined as the body factor $m=d\varphi_S/dV_{GS}$) can be larger than 1, so that SS<2.3 k_BT in this case. Fig. S9c shows that *m* varies with V_{GS} for different t_f. It can be seen that m>1 in the subthreshold regime for a MoS₂ NC-FET and m enlarges when t_f increases for a given V_{GS}. It causes that SS can be smaller 60 mV/dec in a big range of I_{DS} as shown in Fig. S9d. The results from our analytical model match well with those from the experimental data, as shown in Fig. 2.

Fig. S9e shows the transfer characteristics of a $MoS_2 NC$ -FET for different V_{DS} . Contrary to the normal MOSFETs, there is a reverse DIBL effect in the transfer characteristics of the MoS_2 NC-FET. That is, the threshold voltage increases when V_{DS} increases. In order to understand this unique property, the V_{mos} varying with V_{GS} for different V_{DS} is shown in Fig. S9f. One observes that V_{mos} reduces when V_{DS} increases in the subthreshold voltage. On the other hand, V_{DS} has almost no impact on I_{DS} of the intrinsic MoS_2 transistor as shown in Fig. S9g. The reason is that while the DIBL effect of a long-channel intrinsic MoS_2 transistor can be neglected, but this is not true for $MoS_2 NC$ -FET where I_{DS} is reduced with increasing V_{DS} .

The NC-FET also exhibits a characteristic negative differential resistance (NDR) in the output characteristics. Fig. S9h illustrate the output characteristics of a MoS₂ NC-FET for different V_{GS} (with $t_f=20$ nm). There is a clear NDR effect when the device works in the saturation region ($V_{DS}>V_{GS}-V_{th}$). Simulated V_{mos} vs V_{DS} curves for different V_{GS} are shown in Fig. 3d. It is seen that V_{mos} decreases when V_{DS} increases when the device works in the saturation region. On the other hand, V_{DS} has a small impact on I_{DS} of the intrinsic MoS₂ transistor when the device works in the

saturation region. Thus, V_{mos} dominates the saturation current of the MoS₂ NC-FET. That is, the saturation current is reduced with increasing V_{DS} .

Although the non-hysteretic conditions have been achieved in steady-state, hysteresis during I_D-V_{GS} measurements can still appear as the result of dynamic dumping factor ρ >0. Because the steady-state model is ideal while the actual measurement process is dynamic because the rise time of the gate voltage cannot be infinity so that V_{mos} cannot follow the change speed of V_{GS}, which leads to the hysteresis (Fig. S10a). If there is no damping constant, as shown in Fig. S10d and S10e, no hysteresis can be observed for a MoS₂ NC-FET with 20 nm HZO. But if we add a dumping resistor (R_{FE} in Fig. S8b) so that ρ is greater than zero, hysteresis will exist again, as shown in Fig. S10b and S10c. Thus, the second origin of hysteresis is the existence of dumping constant in the ferroelectric HZO.

Based on the discuss above, the hysteresis measured in this work is mostly dumping constant induced hysteresis, as shown in Fig. 2c in manuscript, which is measurement speed dependent. Therefore, our devices fulfill the condition of DC non-hysteretic and internal gain conditions. Meanwhile, by comparing the simulation results on parasitic capacitance, it can be concluded that the damping constant is the origin of the hysteresis and the parasitic capacitance causes the negative DIBL effect, as shown in Fig. S10b-e. And our experimental results in Fig. 3a in the manuscript qualitatively match with simulation results in Fig. S10. The experimental measured dumping factor is $\rho \sim 30 \ \Omega m$ for ferroelectric HZO¹⁸, which is used in this work for the prediction of working speed for MoS₂ NC-FETs shown in Fig S10f. It can be seen that the MoS₂ NC-FETs still maintain decent hysteresis up to 0.1-1 MHz.



Figure S8 | Experiments and simulations of the internal gain and non-hysteretic conditions on MoS₂ NC-FETs. a Cross-section view of the MoS₂ NC-FET in simulation. b Simplified small-signal capacitance representation of a MoS₂ NC-FET for steady-state and dynamic simulation. C_{2D} is the capacitance of MoS₂ channel, C_{ox} is the capacitance of the Al₂O₃ layer, and C_{FE} is the capacitance of HZO layer. c Experimental polarization-voltage measurement on ferroelectric HZO with MIM structure (TiN/HZO/TiN). d I_D-V_{GS} characteristics for MoS₂ NC-FET as in Fig. 2a and the simulation based on parameters extracted from Fig. S8c. c Comparison of C⁻¹ between C_{eq} , C_{device} and $|C_{FE}|$, which shows $|C_{FE}|>C_{device}$ to fulfill non-hysteretic condition and $|C_{FE}|<C_{eq}$ to fulfill internal gain condition. d I_D-V_{GS} characteristics at V_{DS} =0.1 V for HZO films with various thicknesses. $|C_{FE}|<C_{device}$ at 100 nm HZO leads to a large hysteresis in steady-state. e SS vs. I_D characteristics at different C_{fr}. f The t_{ox}-t_f design plane of the MoS₂ NC-FET. The boundary line represents the capacitance match: $-C_{FE}=C_{device}$.



Figure S9 | Simulation of negative DIBL and NDR effect on MoS₂ NC-FETs. a I_D -V_{GS} characteristics of MoS₂ NC-FETs with HZO thickness from 0 nm to 40 nm. b Interfacial potential vs. V_{GS} with HZO thickness from 0 nm to 40 nm. c DC voltage gain of MoS₂ NC-FETs with HZO thickness from 0 nm to 40 nm. d SS-I_D characteristics of MoS₂ NC-FETs with HZO thickness from 0 nm to 40 nm. e I_D -V_{GS} characteristics of MoS₂ NC-FETs at different V_{DS}. f Interfacial potential vs. V_{GS} of the same MoS₂ NC-FET at different V_{DS}. g I_D -V_{GS} characteristics of MoS₂ FETs with no HZO dielectrics at different V_{DS}. h I_D -V_{DS} characteristics of MoS₂ NC-FETs at different V_{GS}. Clear NDR can be observed at low V_{GS}.



Figure S10 | Simulation on stability and the effects of parasitic capacitance and dumping constant. a Simulated transient behavior of a MoS₂ NC-FET. V_{mos} cannot follow the change of V_{GS} , which leads to the hysteresis. b I_D - V_{GS} characteristics with damping constant and parasitic capacitance for different V_{DS} . c I_D - V_{GS} characteristics with damping constant and parasitic capacitance for different V_{DS} . d I_D - V_{GS} characteristics without damping constant and without the parasitic capacitance for different V_{DS} . d I_D - V_{GS} characteristics without damping constant and with the parasitic capacitance for different V_{DS} . e I_D - V_{GS} characteristics without damping constant and without the parasitic capacitance for different V_{DS} . e I_D - V_{GS} characteristics without damping constant and without the parasitic capacitance for different V_{DS} . f I_D - V_{GS} characteristics for a MoS₂ NC-FET at different frequencies.

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