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Mechanisms of current fluctuation in ambipolar black phosphorus field-effect transistors

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Multi-layer black phosphorus has emerged as a strong candidate owing to its high carrier mobility with most of the previous research work focused on its p-type properties. Very few studies have been performed on its n-type electronic characteristics which are important not only for the complementary operation for logic, but also crucial for understanding the carrier transport through the metal–black phosphorus junction. A thorough understanding and proper evaluation of the performance potential of both p- and n-types are highly desirable. In this paper, we investigate the temperature dependent ambipolar operation of both electron and hole transport from 300 K to 20 K. On-currents as high as 85 μA μm^{-1} for a 0.2 μm channel length BP nFET at 300 K are observed. Moreover, we provide the first systematic study on the low frequency noise mechanisms for both n-channel and p-channel BP transistors. The dominated noise mechanisms of the multi-layer BP nFET and pFET are mobility fluctuation and carrier number fluctuations with correlated mobility fluctuations, respectively. We have also established a baseline of the low electrical noise of 8.1×10^{-9} μm^2 Hz^{-1} at 10 Hz at room temperature for BP pFETs, which is 3 times improvement over previous reports, and 7.0×10^{-8} μm^2 Hz^{-1} for BP nFETs for the first time.

Introduction

The discovery of graphene has triggered tremendous scientific interest on various two-dimensional (2D) materials.[1] An important advantage of 2D materials is a greatly improved short channel effect at the scaling limit due to their atomically thin channel.[2] Despite the excellent mobility of graphene, its gapless nature severely limits its potential for applications in logic circuits.[3] Semiconducting transition metal dichalcogenides (TMDs) with a sizeable bandgap, such as MoS_2, have attracted much attention due to their excellent electronic properties.[2,4–7] High frequency, logic circuits and amplifiers with high gain as well as sensing properties have been demonstrated.[8–13] Recently, black phosphorus (BP) has been found to be a layered material with a tunable bandgap ranging from ~0.3 to ~2.0 eV.[14–18] Field-effect transistors (FETs) based on few-layer BP show encouraging results with high hole mobility up to 1000 cm^2 V^{-1} s^{-1} and even higher with hexagonal boron nitride passivation.[15,16,19–22] However, despite the progress made in high-performance BP pFETs by several groups,[15,16,18,22–24] detailed research on the output performance and limits of BP nFETs is still lacking, which is key to realize complementary metal–oxide semiconductor (CMOS) and functional circuits. In addition, the potential to operate in ambipolar regions in the BP transistors could make it ideal for CMOS applications which could greatly reduce the process complexity and cost.[25–27] Moreover, BP transistors, similar to other 2D semiconductors, suffer from high contact resistance (R_c), which plays an important role not only in output current as studied by many, but also in its noise floor, which determines the signal to noise ratio and remains an important target for every technology node on the CMOS roadmap. As a result, it becomes critical to understand the metal–BP contact and its impact on the ambipolar electronic transport and associated noise behavior. The current fluctuation represented by the noise measurement has been studied on two dimensional materials such as graphene and MoS_2,[12,28–39] but there has only been one such study on BP transistors published very recently, which only focused on the pFET operation.[40] As discussed above, it is imperative to understand both the electrical performance and transport mechanisms of n-channel and p-channel of BP based devices. Thus, the systematic temperature dependent study of noise behavior and mechanisms of the BP nFET, and its comparison with that of the pFET, as we addressed in this work, serves as a necessary part for better understanding the BP ambipolar transistors. In this paper, we demonstrate hole and electron transport as well as the

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low-frequency noise in multi-layer BP nFETs and pFETs from 300 to 20 K. The contact resistance of nFETs is much larger than that of pFETs, which limited its performance, including drain current and noise level. We also observe that the dominated 1/*f* noise mechanism of multi-layer BP nFETs and pFETs are mobility fluctuation and carrier number fluctuations with correlated mobility fluctuations, respectively.

Experimental

In the experiments, the 90 nm SiO_2 and p^{++} Si were used as gate dielectric and back gate, respectively. Multi-layer BP were exfoliated from the bulk crystal black phosphorus (Smart-elements), and then transferred to a 90 nm SiO_2 substrate. All samples were sequentially cleaned with acetone, methanol, and isopropanol to remove the Scotch tape residues, and then stored under a nitrogen atmosphere. E-beam lithography was used to define the source and drain patterns, using a Vistec VB6. 30/50 nm Ni/Au was deposited using e-beam evaporation under 10^{-6} Pa pressure, with a deposition rate of 1 Å s^{-1}. No annealing was performed after the deposition of the metal contacts. The 8 nm top passivation was deposited of by an ASM F-120 ALD system at 200 °C, using trimethylaluminum (TMA) and H_2O as precursors. Before ALD deposition, a 2 nm Al thin layer was pre-deposited as the seeding film.

Results and discussion

The BP transistor structure is depicted in Fig. 1(a). Fig. 1(b) shows an image of the arrayed BP devices measured by atomic force microscopy (AFM), with the channel lengths ranging from 0.1 μm to 2 μm. An Al_2O_3 capping layer deposited by atomic layer deposition is used to protect the BP FETs. The thickness of BP used in this work is 8.6 nm, as shown in Fig. 1(c), measured by AFM.

Fig. 2(a) shows transfer characteristics ($I_d - V_g$) of the BP device with the channel length L = 2 μm at 300 and 20 K. The device exhibits clear ambipolar behavior. I_{on}/I_{off} of about 3.3 × 10^3 and 1.3 × 10^3 at V_d = −0.05 V are obtained for the BP pFET and nFET at 300 K, respectively. When the temperature decreases to 20 K, the off current decreases significantly and the I_{on}/I_{off} is over 10^6 for both branches. When the channel length scales to 0.2 μm as shown in Fig. 2(b), the drain current I_d increases about 4 times. In addition, the I_{on}/I_{off} for the pFET decreases to 120 at 300 K due to drain induced barrier lowering (DIBL), where the drain bias decreases the source-end barrier, and increases the off-state current.[41] Fig. 2(c) shows the output characteristics of the 0.2 μm device with V_d sweeping from 0 to 2 V for the nFET and 0 to −2 V for the pFET. At 300 K, the maximum drain current (I_d) for the BP nFET and pFET are 85 and 188 μA $μm^{-1}$, respectively, which is already quite competitive in thin film transistor applications under CMOS operation.[42] Note here that the nFET output current exceeds the best of previous reports by a factor of two.[43] When

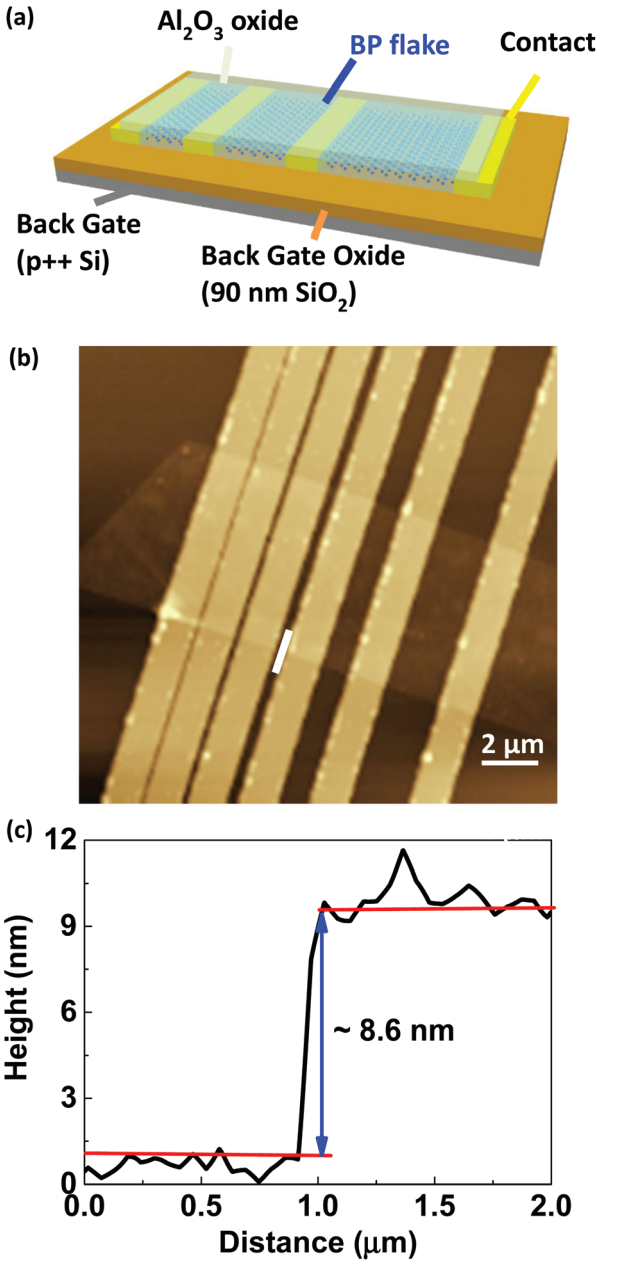

Fig. 1 (a) A schematic and (b) AFM images of the multi-layer BP device. The scale bar is 2 μm. (c) The BP flake with a measured thickness of 8.6 nm by AFM.

the temperature decreases to 20 K as shown in Fig. 2(d), while the drain current of the pFET increases, it decreases for the nFET, indicating different carrier transport mechanisms.

To fully harness the unique properties of BP, a quantitative analysis of the contact resistance between BP and the metal becomes very important. The contact resistance for both BP nFET and pFET are extracted from the transfer length method (TLM) as shown in Fig. 3(a). We can see that in Fig. 3(b), a clear dependence on the back gate bias is observed for the contact resistance at all temperatures and the contact

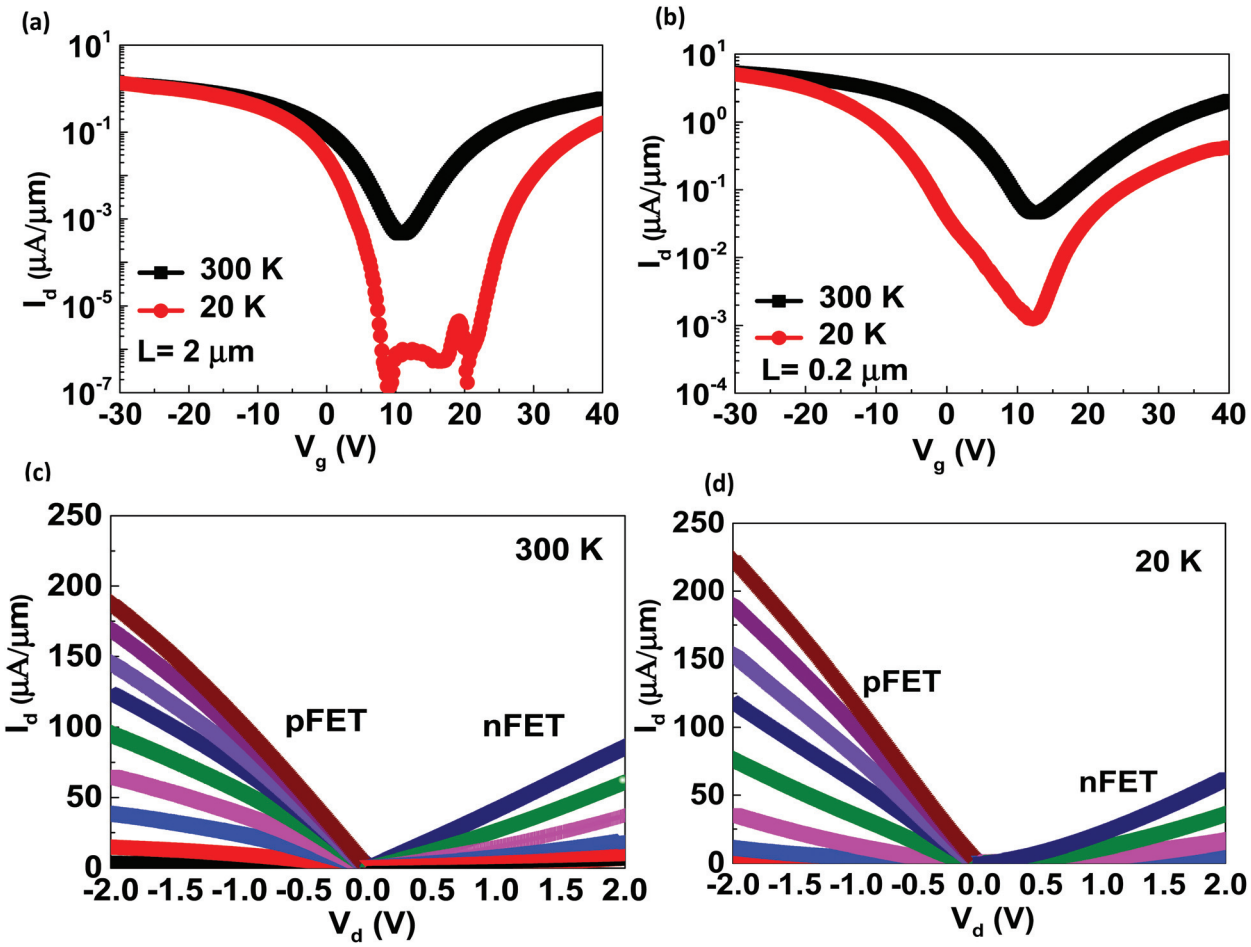

Fig. 2 Transfer characteristics of the BP ambipolar transistor with V_d = −0.05 V at 300 K and 20 K for (a) 0.2 μm and (b) 2 μm. Output characteristics of the 0.2 μm device at (c) 300 K and (d) 20 K. For the pFET, V_g is from 10 to −30 V with a step of −5 V. For the nFET, V_g is from 15 to 40 V with a step of 5 V.

resistance increases at lower temperatures, indicating the dominant thermionic injection of the Schottky barrier formed at metal–BP contacts. At 300 K, the smallest R_c determined in the Ni/BP junction for the hole branch is 4.2 kΩ μm at V_g = −30 V and 6.9 kΩ μm at V_g = 10 V, while for the electron branch, the R_c is 10.5 kΩ μm at V_g = 40 V and 38.5 kΩ μm at V_g = 30 V. The R_c of BP FETs at the p-side is smaller than that of the n-side, which is due to the fact that the Ni metal Fermi level is closer to the valence band. The field-effect mobility μ_{FE} is extracted in the linear region of the transfer characteristics from the 2 μm device according to the following equation $\mu_{FE} = g_m/(C_gEW)$, where L and W are the length and width of the channel, respectively, C_g is the gate capacitance (38.34 nF cm^{-2} for the 90 nm SiO_2 layer), E is the transverse electric field in the channel ($E = (V_d - 2R_cI_d)/L$), and g_m is the transconductance.[44] Fig. 3(b) shows the electron and hole mobilities as a function of temperature from the same BP FET operating as nFET and pFET, respectively. The electron and hole mobilities are 47 and 65 cm^2 V^{-1} s^{-1}, respectively, which is similar to the previously reported BP FETs with passivation at room temperature.[24,45] The increase of electron and hole mobilities with decreasing temperature is observed, which can be attributed to the reduced phonon scattering from the underlying substrate. It should be noted that the drain current decreases with temperature for the BP nFET, which is mainly attributed to the increase in contact resistance at low temperature.

It is well known that low-frequency noise is a powerful tool to obtain a global view about the noise behavior and performance of the devices and the quality of their interfaces, and more importantly, the effect of contact as in this case. We performed low frequency noise measurements on the BP nFET and pFET in the linear region at V_d = 0.2 V from 300 to 20 K on the 2 μm device. The thickness of the BP flake is 8.6 nm as shown in Fig. 1(c). Normalized noise power spectra (S_{id}/I_d^2) of the BP pFET for four different gate voltages between 1 Hz and 1 kHz at 300 K are shown in Fig. 4(a). The noise spectra follow the typical 1/f dependence and can be quantitatively characterized by $S_{id} = \frac{AI_d^2}{f^\gamma}$, where S_{id} is the current noise power spectral density, f is the frequency, I_d is the current through the device

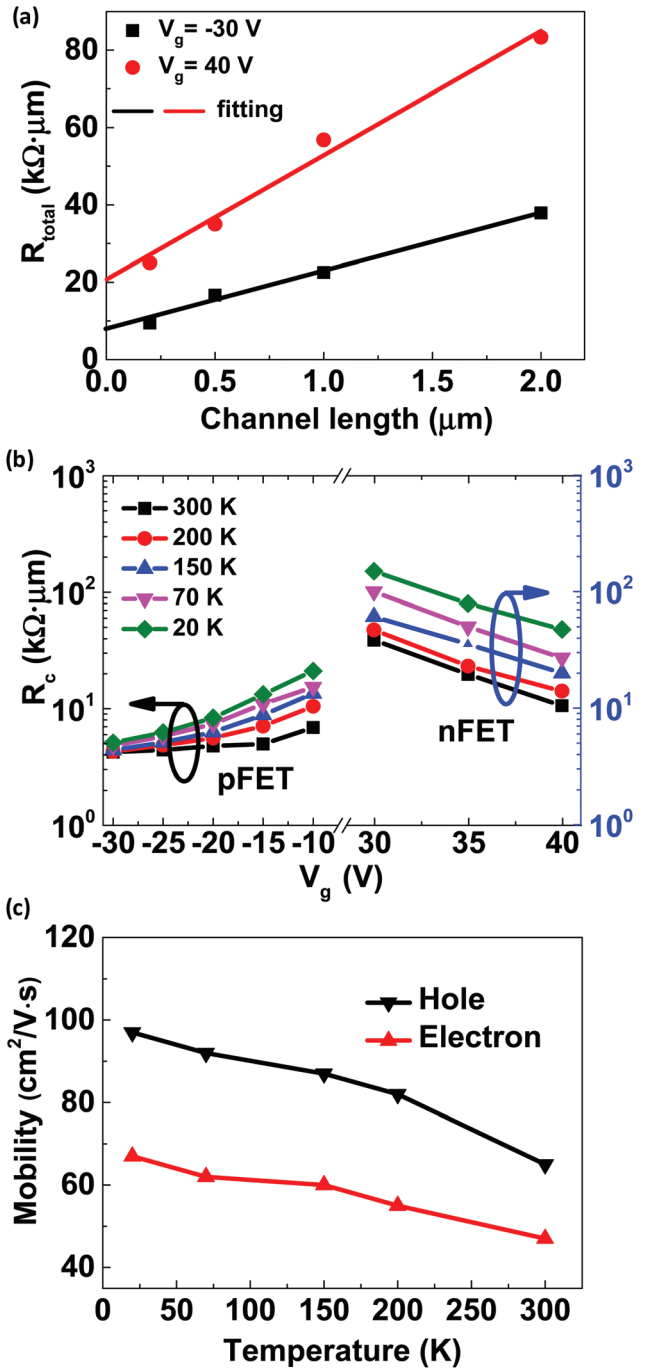

Fig. 3 (a) Contact resistance as a function of back gate voltage extracted from $I_d - V_d$ curves of the BP nFET and pFET at different temperatures. (b) Mobility as a function of temperature for the BP nFET and pFET.

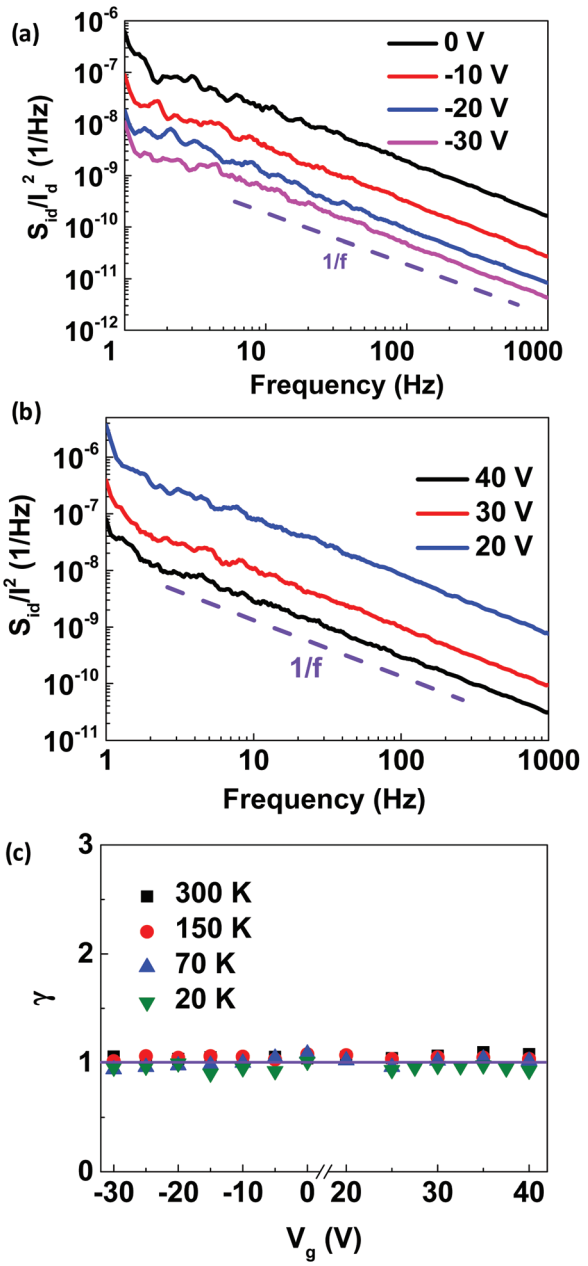

Fig. 4 Drain current spectral density (S_{id}/I_d^2) as a function of frequency at various back gate voltages at 300 K for (a) pFET and (b) nFET. (c) Frequency exponent as a function of back gate voltage from 300 to 20 K for the same device as shown in (a) and (b).

channel, γ is the frequency exponent, and A is the noise amplitude.[46,47] It can be seen that with decreasing V_g from 0 to −30 V, the noise magnitude decreases monotonically with a factor of 40. Fig. 4(b) shows the noise characteristics of the BP nFET in the same device at 300 K, which exhibits the same $1/f$ trend. The extracted frequency exponent γ as a function of V_g at all temperatures is plotted in Fig. 4(c). The γ is between 0.9 and 1.1 as determined from a least-squares fit, which shows little dependence on the back gate voltage and temperature.

To investigate the noise mechanism, S_{id}/I_d^2 at f = 100 Hz and the corresponding $(g_m/I_d)^2$ at 300 K as a function of drain current for the BP pFET and nFET are plotted in Fig. 5(a) and (b), respectively. Fig. 5(a) shows the S_{id}/I_d^2 and the corresponding $(g_m/I_d)^2$ of the BP pFET at f = 100 Hz as a function of drain current at 300 K. We can see that the S_{id}/I_d^2 and the corresponding $(g_m/I_d)^2$ follow the same trend over a wide drain current range. This indicates that the carrier number fluctu-

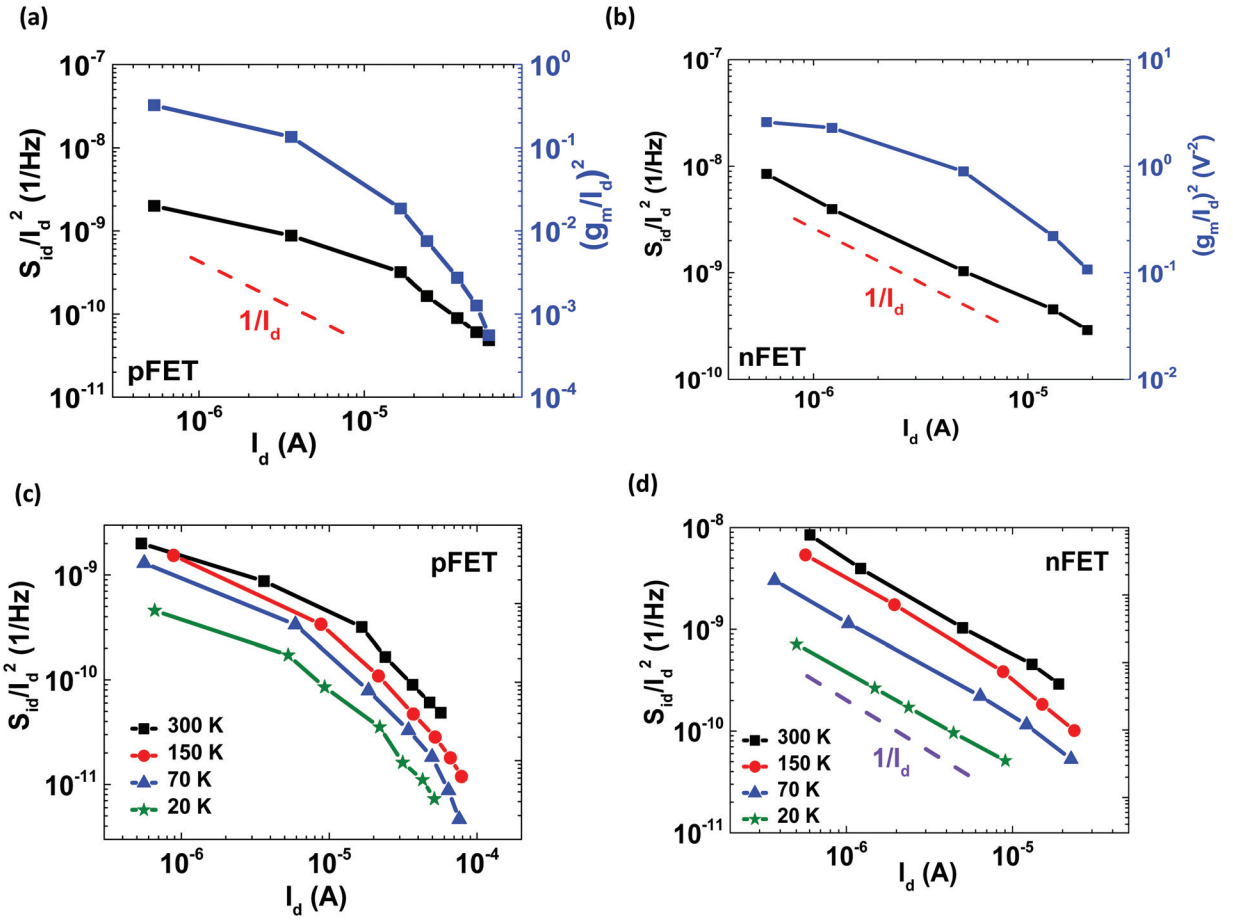

Fig. 5 Normalized drain current noise spectral density (S_{id}/I_d^2) and the transconductance to drain current ratio squared [$(g_m/I_d)^2$] at V_d = 0.2 V and f = 100 Hz *versus* drain current at 300 for the BP (a) pFET, (b) nFET. Normalized drain current noise spectral density (S_{id}/I_d^2) at V_d = 0.2 V and f = 100 Hz as a function of drain current from 300 to 20 K for the BP (c) pFET, (d) nFET.

ation model is responsible for the BP pFET device.[47,48] The departure of the noise level from the $(g_m/I_d)^2$ observed at strong inversion can be attributed to correlated mobility fluctuations.[48–50] This is consistent with the previous reports on few-layer BP pFETs.[40] Meanwhile, for the nFET as shown in Fig. 5(b), it is clear that there is substantial deviation between the S_{id}/I_d^2 and the $(g_m/I_d)^2$ over a broad drain current range. And the observed S_{id}/I_d^2 follows the $1/I_d$ trend, indicating that a mobility fluctuation model governs.[47,48] It is noted here that this behavior is very different from what is observed from previous pFETs. To further investigate the mechanisms, Fig. 5(c) shows that S_{id}/I_d^2 curves of pFETs at low temperatures also exhibit the same trend as in 300 K. In the pFET, low frequency noise originates from the trapping and releasing of the carrier near the BP/SiO_2 interface which dominates the noise mechanism. On the other hand, as shown in Fig. 5(d), S_{id}/I_d^2 at f = 100 Hz as a function of drain current from 300 to 20 K for the BP nFET, all follow the $1/I_d$ trend in the whole range, indicating the temperature independent noise mechanism. In the nFET, the main noise model is mobility fluctuation induced by lattice and impurity scattering. It has been previously reported that the Al_2O_3 passivation layer deposited at low temperature contains large amounts of positive fixed charge, inducing an ambipolar behavior and decreasing the hole mobility of BP pFETs.[26] Therefore, it is likely that the $1/f$ noise source in the nFET is from the electron impurity scattering centers in the interface with the Al_2O_3 capping layer. In addition, the magnitude of noise amplitude of the nFET and the pFET decreases with decreasing temperature, indicating a thermal activated process.

The $1/f$ noise in the homogeneous layers can be characterized by a parameter α_H using Hooge's empirical formula: $\frac{S_{id}}{I_d^2} = \frac{\alpha_H}{fN}$, where α_H is the Hooge parameter, N is the total number of carriers. In the linear region (V_d = 0.2 V) under gate overdrive conditions $V_g - V_{th} > 0$, N can be approximated as $N = (V_g - V_{th})LWC_g/e$, where C_g is the gate capacitance per unit area (38.34 nF cm^{-2} for the 90 nm SiO_2 layer), e is the elemental charge, and L and W are the channel length and width, respectively.[47] The extracted Hooge parameter α_H of the 2 μm device at various temperatures is shown in Fig. 6(a), exhibiting clear temperature dependence. At 300 K, the α_H values of the

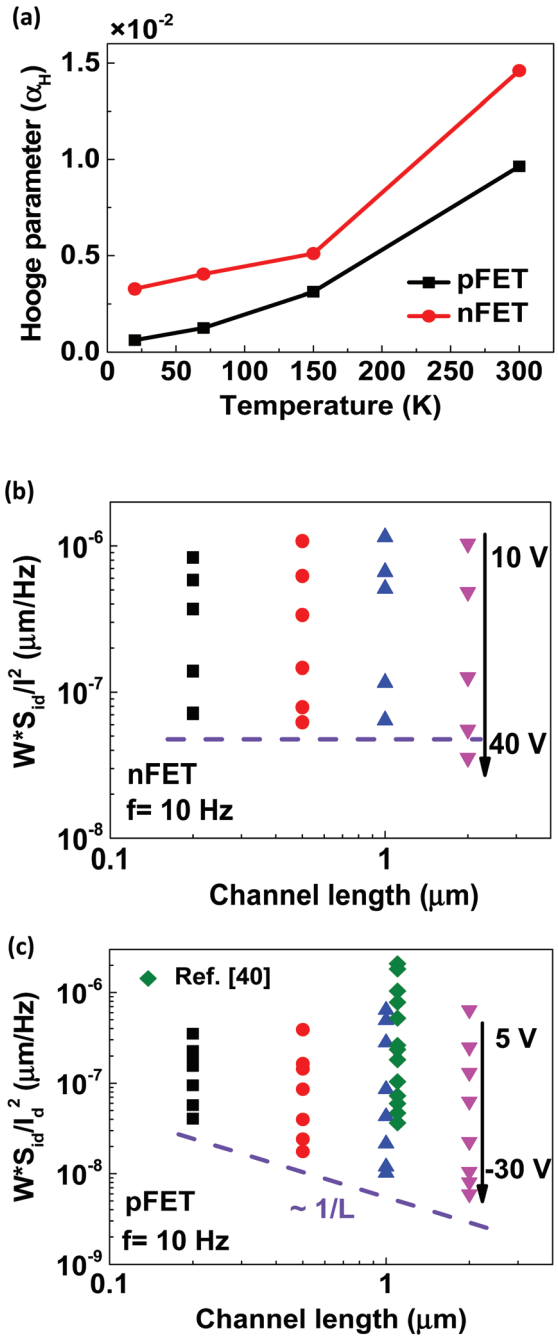

Fig. 6 (a) Hooge parameter α_H from 300 to 20 K for the BP nFET and pFET. Normalized current spectral density $W \times S_{id}/I_d^2$ *versus* channel length for different BP transistors at 300 K in this work for (b) nFETs, (c) pFETs. The results from ref. 40 are added for comparison.

BP nFET and pFET are 1.4×10^{-2} and 9.6×10^{-3}, respectively. When decreasing the temperature down to 20 K, the values change to 3.3×10^{-3} and 6.0×10^{-4} accordingly. This confirms that the performance of the BP nFET is inferior to that of the pFET, which is consistent with the electrical results. To study the scaling of $1/f$ noise, the typical $W \times S_{id}/I_d^2$ at $f = 10$ Hz of the BP nFET and pFET as a function of channel length at 300 K when sweeping the gate voltage V_g from weak to strong inversion is shown in Fig. 6(b) and (c). For the nFET in Fig. 6 (c), $1/f$ noise decreases with increasing gate voltage and is independent of channel length, which is mainly attributed to the contact dominated transport at strong inversion as stated in Fig. 3(a). The lowest noise level at $f = 10$ Hz at 300 K is 7.0×10^{-8} μm^2 Hz^{-1} for the nFET. For the pFET in Fig. 6(c), at threshold gate voltage, the $1/f$ noise is large and independent of the channel length. With increasing the gate voltage to the strong inversion region ($V_g = -30$ V for the pFET), the noise level decreases over one order of magnitude and shows strong dependence on the channel length. This indicates that the noise from the source/drain contact makes a significant contribution at the threshold regime, while the channel noise dominates in the strong inversion region for the pFET.[51] At the same time, we compare the noise level of the BP pFET in this work with other BP pFET results in the literature.[40] The low frequency noise at $f = 10$ Hz at room temperature is as low as 8.1×10^{-9} μm^2 Hz^{-1}, which is about 3 times reduction over the previous reports.

Conclusion

In conclusion, we investigated the ambipolar output current and noise properties of the multi-layer BP transistors from 300 to 20 K. The contact resistance and mobility of the multi-layer BP nFET and pFET are studied and their impact on output characteristics are discussed. The low frequency noise mechanisms of the multi-layer BP nFET and pFET are found to be mobility fluctuation and carrier number fluctuation with correlated mobility fluctuation, respectively. These results not only demonstrated high performance ambipolar operation based on multi-layer BP transistors with low noise, but also provide fundamental insights into the electron and hole transport and related $1/f$ mechanisms at various temperatures.

Conflict of interest

The authors declare no competing financial interest.

Acknowledgements

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