Supplementary Information for:

Scaling of Atomic-Layer-Deposited Atomically Thin Indium Oxide Transistors

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1. Characteristics of Ultrathin In_2O_3 Transistors

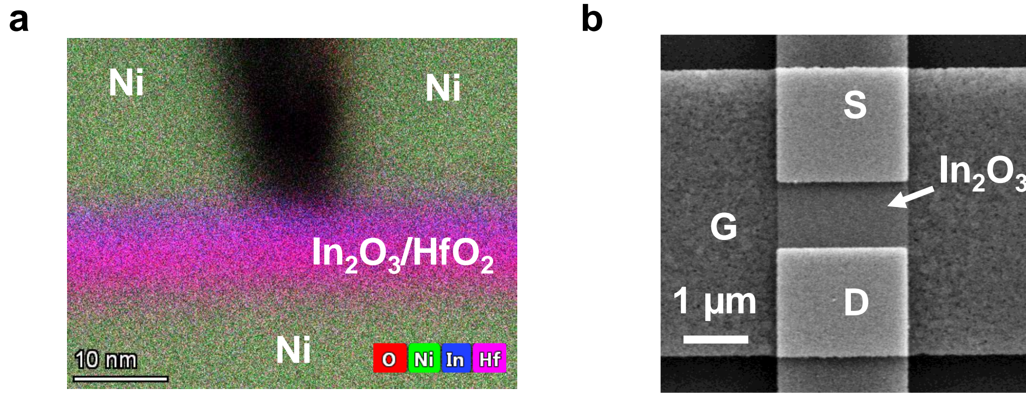

Figure S1. a, TEM cross-sectional image with EDX element mapping (O, Ni, In and Hf) of an In_2O_3 transistor with L_{ch} of 8 nm, T_{ch} of 3.5 nm and 3 nm HfO_2 as gate insulator. **b,** SEM image from top view of a typical long channel device with a channel width of 2 μm defined by dry etching.

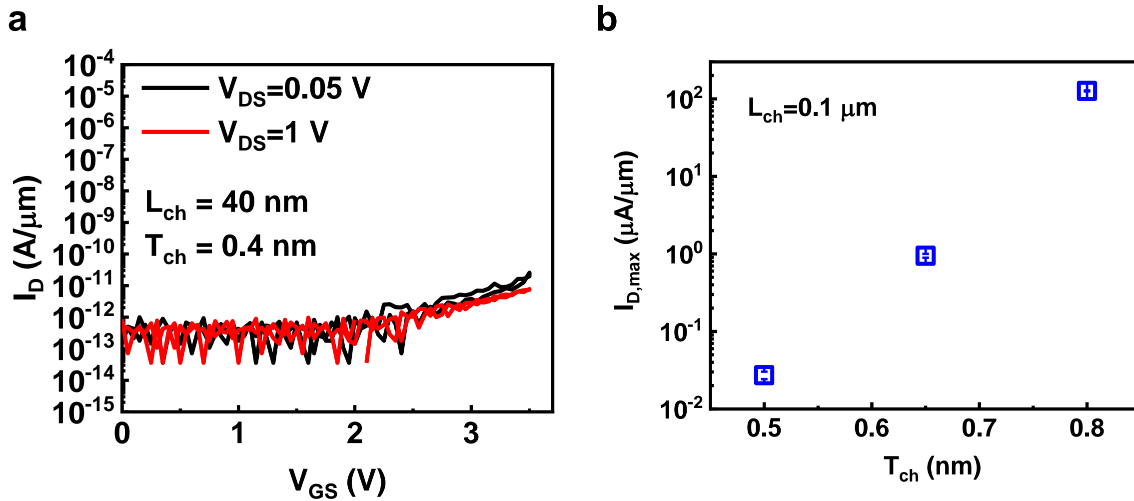

Figure S2. a, I_D-V_{GS} characteristics of a representative ALD In_2O_3 transistor with L_{ch} of 40 nm, T_{ch} of 0.4 nm and 5 nm HfO_2 as gate insulator. **b,** $I_{D,max}$ versus T_{ch} characteristics for ALD In_2O_3 transistors extracted from Fig. 2g.

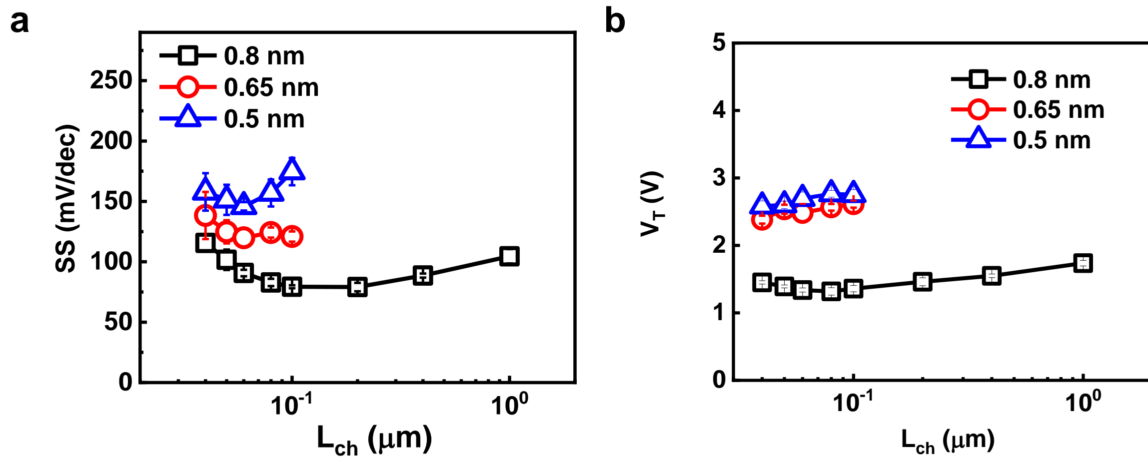

Figure S3. a, SS and **b,** V_T scaling metrics of ALD In_2O_3 transistors with different T_{ch} and with 5 nm HfO_2 as gate insulator.

2. C-V Characterization of the Gate Stack Capacitor

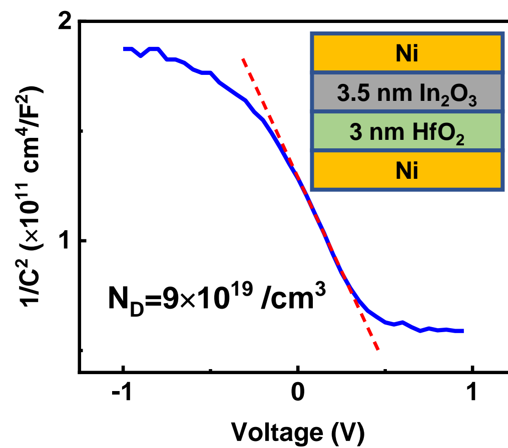

Figure S4. $1/C^2$ versus voltage characteristics of a MOS capacitor with Ni/3 nm HfO_2/3.5 nm In_2O_3/Ni stack.

3. Benchmarking of ALD In_2O_3 Transistors

Table I. Performance of State-of-the-Art Transistors with Ultrathin Semiconducting Channel

Material	Thickness (nm)	L_{ch} (nm)	$I_{D,max}$ (A/μm)	g_m (S/μm)	mobility ($cm^2/V\cdot s$)	R_C (kΩ·μm)	Reference
ITO	4	40	5.20E-04	5.50E-04	-	-	[1]
ITO	4	100	8.50E-04	-	-	-	[1]
ITO	10	200	1.15E-03	-	-	-	[1]
ITO	3.5	10	1.86E-03	1.05E-03	40	0.162	[2]
IGZO	3.6	38	3.50E-04	1.25E-04	34	-	[3]
IGZO	61.3	100	1.30E-03	6.12E-04	-	-	[4]
IGZO	15	27	1.10E-04	1.74E-04	-	-	[5]
IWO	7	100	5.00E-04	-	20	1.2	[6]
MoS_2	0.65	35	1.14E-03	-	20	0.123	[7]
MoS_2	3.8	80	8.30E-04	-	51	0.54	[8]
MoS_2	4	10	5.20E-04	1.42E-04	-	-	[9]
MoS_2	5	100	4.60E-04	-	55	0.5	[10]
MoS_2	0.65	380	7.00E-04	-	33.5	0.48	[11]
MoS_2	0.65	100	3.90E-04	-	-	1.1	[12]
MoS_2	1.95	70	3.70E-04	1.00E-04	6	1.8	[13]
MoS_2	0.65	500	4.50E-04	-	102.6	-	[14]
MoS_2	2.6	2000	2.71E-04	-	22	2.2	[15]
MoS_2	3.3	2000	2.04E-04	-	25	-	[15]
BP	14.9	200	1.04E-03	-	-	-	[16]
BP	12.5	100	1.20E-03	-	-	-	[17]
BP	8	200	8.50E-04	3.40E-04	144	0.58	[18]
WS_2	1.3	100	3.10E-04	3.20E-04	20	-	[19]
WS_2	2.1	40	7.00E-04	-	-	0.5	[20]

References

1. Li, S. *et al.* Nanometre-thin indium tin oxide for advanced high-performance electronics. *Nat. Mater.* **18**, 1091–1097 (2019).

2. Li, S., Gu, C., Li, X., Huang, R. & Wu, Y. 10-nm Channel Length Indium-Tin-Oxide transistors with I_{on} = 1860 μA/μm, G_m = 1050 μS/μm at V_{ds} = 1 V with BEOL Compatibility. in *IEEE Int. Electron Devices Meet.* 905–908 (IEEE, 2020).

3. Samanta, S. *et al.* Amorphous IGZO TFTs featuring Extremely-Scaled Channel Thickness and 38 nm Channel Length : Achieving Record High $G_{m,max}$ of 125 µS/µm at V_{DS} of 1 V and I_{ON} of 350 µA/µm. in *IEEE Symposium on VLSI Technology* TH2.3 (IEEE, 2020).

4. Han, K. *et al.* First Demonstration of Oxide Semiconductor Nanowire Transistors: a Novel Digital Etch Technique, IGZO Channel, Nanowire Width Down to ~20 nm, and I_{on} Exceeding 1300 µA/µm. in *IEEE Symposium on VLSI Technology* (IEEE, 2021).

5. Matsubayashi, D. *et al.* 20-nm-Node trench-gate-self-aligned crystalline In-Ga-Zn-Oxide FET with high frequency and low off-state current. in *IEEE Int. Electron Devices Meet.* 141–144 (IEEE, 2015).

6. Chakraborty, W. *et al.* BEOL Compatible Dual-Gate Ultra Thin-Body W-Doped Indium-Oxide Transistor with I_{on} = 370μA/μm, SS = 73mV/dec and I_{on}/I_{off} ratio > $4x10^9$. in *Symposium on VLSI Technology* TH2.1 (IEEE, 2020).

7. Shen, P. C. *et al.* Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).

8. Liu, Y. *et al.* Pushing the Performance Limit of Sub-100 nm Molybdenum Disulfide Transistors. *Nano Lett.* **16**, 6337–6342 (2016).

9. Yang, L., Lee, R. T. P., Rao, S. S. P., Tsai, W. & Ye, P. D. 10 nm nominal channel length MoS_2 FETs with EOT 2.5 nm and 0.52 mA/μm drain current. in *2015 73rd Annual Device Research Conference (DRC)* 237–238 (IEEE, 2015).

10. Lingming Yang *et al.* High-performance MoS_2 field-effect transistors enabled by chloride doping: Record low contact resistance (0.5 kΩ·µm) and record high drain current (460 µA/µm). in *IEEE Symposium on VLSI Technology* 192–193 (IEEE, 2014).

11. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High Current Density in Monolayer MoS_2 Doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).

12. Chou, A.-S. *et al.* High On-Current 2D nFET of 390 μA/μm at V_{DS} = 1V using Monolayer CVD MoS_2 without Intentional Doping. in *IEEE Symposium on VLSI Technology* TN1.7 (IEEE, 2020).

13. Krasnozhon, D., Dutta, S., Nyffeler, C., Leblebici, Y. & Kis, A. High-frequency, scaled MoS_2 transistors. in *IEEE Int. Electron Devices Meet.* 703–706 (IEEE, 2015).

14. Li, T. *et al.* Epitaxial growth of wafer-scale molybdenum disulfide semiconductor single crystals on sapphire. *Nat. Nanotechnol.* (2021).

15. Kang, J., Liu, W. & Banerjee, K. High-performance MoS_2 transistors with low-resistance molybdenum contacts. *Appl. Phys. Lett.* **104**, 2–7 (2014).

16. Si, M., Yang, L., Du, Y. & Ye, P. D. Black phosphorus field-effect transistor with record drain current exceeding 1 A/mm. in *2017 75th Annual Device Research Conference (DRC)* (IEEE, 2017).

17. Li, X. *et al.* High-speed black phosphorus field-effect transistors approaching ballistic limit. *Sci. Adv.* **5**, eaau3194 (2019).

18. Yang, L. M. *et al.* Few-layer black phosporous PMOSFETs with BN/Al_2O_3 bilayer gate dielectric: Achieving I_{on}= 850 µA/µm, g_m= 340 µS/µm, and R_c=0.58 kΩ·µm. in *IEEE Intl. Electron Devices Meet.* 127-130 (IEEE, 2016).

19. Lin, D. *et al.* Scaling synthetic WS_2 dual-gate MOS devices towards sub-nm CET. in *IEEE Symposium on VLSI Technology* (IEEE, 2021).

20. Pang, C.-S., Wu, P., Appenzeller, J. & Chen, Z. Sub-1nm EOT WS_2 -FET with I_{DS} > 600µA/µm at V_{DS} =1V and SS < 70mV/dec at L_G =40nm. in *IEEE Int. Electron Devices Meet.* 43–46 (IEEE, 2020).