First Demonstration of Ge Nanowire CMOS Circuits: Lowest SS of 64 mV/dec, Highest g_{max} of 1057 μS/μm in Ge nFETs and Highest Maximum Voltage Gain of 54 V/V in Ge CMOS inverters

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I. Abstract

Ge nanowire CMOS circuits are experimentally demonstrated on a Ge on insulator (GeOI) substrate for the first time. The nanowire CMOS devices have channel lengths (L_{ch}) from 100 to 40 nm, nanowire height (H_{NW}) of 10 nm and nanowire widths (W_{NW}) from 40 to 10 nm, and dielectric EOTs of 2 and 5 nm. Four types of Ge MOSFETs: accumulation mode (AM) and inversion mode (IM) nFETs and pFETs are studied in great details. Record low SS of 64 mV/dec and high maximum trans-conductance (g_{max}) of 1057 μS/μm are obtained on Ge nanowire nFETs. Furthermore, hybrid Ge nanowire CMOS with AM nFET and IM pFET is also first realized. The highest maximum voltage gain reaches 54 V/V.

II. Introduction

As one of the most promising candidates for post-Si CMOS, Ge is intensively studied in the past decade regarding interfaces [1-3], contacts [4-5], scaling [5-8] and 3D channel structures [9-11]. Meanwhile, Ge planar and FinFET CMOS circuits have been realized on GeOI [7] or poly-Ge substrate [8]. However, to minimize the short channel effects (SCE) at 7 nm node and beyond, 3D nanowire channel might be needed, which has the best immunity to SCEs.

In this work, we have successfully realized suspended Ge nanowires by a combination of dry etching and selective wet etching process. The channel area in the nanowire is carefully recessed with an optimized height of 10 nm. The nanowires are further fabricated into both nFETs and pFETs, and then integrated into the *first Ge 3D nanowire CMOS circuits*. To our best knowledge, it's also the first non-Si nanowire CMOS circuits by the top-down approach. To explore Ge CMOS in more details, both AM and IM operation modes are studied on nFETs and pFETs. Ge hybrid CMOS [12] combined of AM nFET and IM pFET has also been successfully demonstrated. The dependences on L_{ch}, W_{NW} and operation mode of the well-behaved nanowire CMOS devices, such as on current (I_{ON}), g_{max}, threshold voltage (V_{TH}), I_{ON}/I_{OFF}, SS, DIBL and maximum voltage gain, are systematically studied.

III. Experiment

Fig. 1 shows the fabrication processes. The experiment started with a GeOI wafer with 90 nm i-type (100) Ge and 400 nm SiO_2 on Si from Soitec™, made by the Smartcut™ technology. After a standard clean (acetone, methanol and isopropanol soaking), the samples were selectively P (5×10^{15} cm^{-2} @ 15 keV) and BF_2 (4×10^{15} cm^{-2} @ 15 keV) implanted for nFETs and pFETs. The energy of both the nFETs' and pFETs' ion implantations is intentionally reduced to keep a low doping concentration in the recessed channel area for AM MOSFETs, due to the thinner 90 nm Ge substrate used in this experiment, as compared to the 180 nm Ge substrate in our previous works [7, 12]. Note that a ZEP 520A mask was used for IM MOSFETs to define the channel length with the smallest L_{ch} of 40 nm, as shown in Fig. 3(a). Following the mesa isolation, an optimized SF_6 dry etching process was applied to form the recessed channel, followed by another common dry etching process to define the fins in the channel region. The nanowire channel release process was carried out using 4% HF solution to selectively remove SiO_2 underneath the Ge nanowire channel. At the same time, the HF soaking could also reduce the surface damages of the nanowires caused by the dry etching process.

For the gate dielectric, 1 nm Al_2O_3 was first grown by ALD at 250 °C and then a post-oxidation process was performed by RTA at 500 °C to form 2 nm GeO_x underneath Al_2O_3, which also activates the n- and p- dopant ions simultaneously. Due to the high diffusivity of P ions inside Ge at high temperature [2, 4], processes with high thermal budget in this experiment were carefully calibrated and simplified. Resulted from that, the common ion activation process was merged with the post oxidation. Next, 8 nm Al_2O_3 was deposited ***only*** for *Chip B* and no Al_2O_3 was deposited on *Chip A*. The overall EOT is calculated to be 2 nm for *Chip A* and 5 nm for *Chip B*. Then, recessed S/D dry etching was conducted by first striping the oxide and then partially removing the top Ge layer in the source/drain region [12]. In following, S/D contact metal was formed by Ni deposition and ohmic annealing. Finally, the gate and interconnection metal was formed by Ni/Au.

All the lithography were carried out by a Vistec EBPG 5200 electron-beam lithography system using pure or diluted ZEP 520A as the resists. In total, 9 steps of lithography process were employed in the device fabrication.

IV. Results and Discussion

Structures:

Fig. 2 illustrates the schematic of the Ge 3D nanowire CMOS and lists the experiment splits and 4 types of MOSFETs fabricated on the same chip. Recessed nanowires are adopted in both AM and IM MOSFETs, aiming at reducing the channel cross sectional area to enhance the gate electrostatic control. The cross sectional cartoon of the middle of nanowire is also given in the inset. The top, left and right side of the nanowire are covered by the gate metal. Therefore, the channel width (W_{ch}) is calculated from $W_{ch} = (2\cdot H_{NW}+W_{NW}) \times$ (number of wires).

The nanowires are patterned in parallel with the main flat of the (100) substrate in the device fabrication. Thus, the carrier transport is in <110> direction [13]. The smallest W_{NW} is 10 nm as shown in Fig. 3(b) and Fig. 3(c) shows the top-down SEM image of a 40 nm W_{NW} nanowire with the smallest L_{ch} of 40 nm. A nanowire array in device gate area is shown in Fig. 3(d) with 40 nm long channel marked. To better illustrate the structures, the gate region is further zoom-out in Fig. 3(e), clearly showing the suspended nanowires with a H_{NW} of 10 nm, as indicated by the inset. The number of wires of pFETs to nFETs is designed to be 11 and 7 for balanced performance and can be adjusted during the mask layout, as shown in Fig. 3(f-g).

Ge nanowire nFETs:

Fig. 4 depicts the transfer curves of a 100 nm L_{ch} and 20 nm W_{NW} AM nFET with an EOT of 2 nm, showing a record low SS of 64.1 mV/dec and I_{ON}/I_{OFF} ratio of 1×10^6 at V_{ds} = 0.05 V. In total, 11 out of 800 fabricated devices in the same chip have SS < 70 mV/dec. It proves the excellent gate control enabled by the nanowire structure, delivering more than 30% and 40% reduced SS over FinFETs and planar MOSFETs. The reduced I_{ON}/I_{OFF} at high V_{ds} is related to the gate induced drain leakage (GIDL) in the device off-state, since the gate leakage current is very low (10 times smaller than the lowest off-state current). Band-gap engineering is needed to suppress the band-to-band tunneling (BTBT) near the drain side to improve the I_{ON}/I_{OFF} ratio.

Fig. 5 shows the SS scaling metrics of 40 nm W_{NW} nFETs at V_{ds} of 0.05 V. Related with gate electrostatic control, devices with longer channel and smaller EOT have lower SS. What's more, IM devices show better SS, due to higher gate electrical fields in the undoped channel [14]. The scale bar is based on ~20 devices measured at each data point. Fig. 6 gives the SS dependence on W_{NW}, showing that smaller nanowire size lowers SS. Fig. 7 shows the mid-gap D_{it} box plot and histogram based on more than 800 devices with L_{ch} = 50~100 nm, extracted from the equation $SS = 60 \times (1 + qD_{it}/C_{ox})$. The mean D_{it} is around 4×10^{12} $eV^{-1}cm^{-2}$ and the lowest value is 7×10^{11} $eV^{-1}cm^{-2}$, indicating a good interface realized by the post oxidation method.

Fig. 8 shows the V_{TH} versus L_{ch} in 2 nm EOT devices, pointing out a small V_{TH} roll-off enabled by the nanowire structure. The AM nFETs are majority carrier devices with n-type dopant in the channel, which makes the devices easier to turn on. Thus, the V_{TH} of AM devices is smaller than that of IM ones. The W_{NW} dependence of V_{TH} is given in Fig. 9 and smaller W_{NW} devices have larger V_{TH} due to better immunity to SCEs. Figs. 10-11 show the DIBL dependences on L_{ch}, W_{NW}, EOT and operation mode. Similar to the case of SS dependence, smaller EOT, W_{NW} and IM devices have smaller DIBLs, owing to better SCE immunity. Fig. 12 shows the I_{ON}/I_{OFF} ratio (V_{ds} = 0.05 V) box plot and histogram based on data points from more than 800 Ge nFETs with various channel lengths. The mean value is around 2×10^5, due to the 3D nanowire structure used.

Figs. 13-15 present the I_d-V_{gs}, g_m-V_{gs} and I_d-V_{ds} curves of a high-performance AM nFET with L_{ch} of 40 nm, W_{NW} of 30 nm and EOT of 2 nm. Thanks to the low EOT and 3D nanowire channel, a record high g_{max} of 1057 μS/μm is obtained at V_{ds} = 1 V and the I_{max} is around 700 μA/μm. Note that recent simulation work [13] indicates that Ge <110> nanowire nFETs could even deliver more current than Si and InAs nFETs. Furthermore, the SS still keeps a low value of 93 mV/dec at such scaled channel length. Fig. 16 gives the I_{ON} scaling metrics of 40 nm W_{NW} devices. Smaller EOT significantly enhances the I_{ON} by 120% at the same V_{gs}-V_{TH}= 1 V. As determined by Fermi-level alignment inside Ge [12], AM nFET would get much higher carrier density compared with IM nFET, as proved by the 25% current improvement. Meanwhile, it's also reported [14] that AM devices would have higher mobility than IM ones. Fig. 17 presents I_{ON} versus W_{NW} for AM nFETs with 2 nm EOT and I_{ON} first increases and then decreases with decreased W_{NW}, which could be related with the tradeoff between cross sectional area, mobility and the self-heating effects [15]. Figs. 18-19 describe the g_{max} versus L_{ch} and W_{NW} for the same sets of devices in Figs. 16-17, showing similar dependence.

Ge nanowire pFETs:

Because of the Fermi-level alignment in Ge [12], IM pFET is preferred for better OFF-state performance since it's harder to move E_F to E_C to turn device OFF in AM pFET with p-type channel. Fig. 20 shows the transfer curves of a 100 nm L_{ch} and 20 nm W_{NW} IM pFET with an EOT of 5 nm. Fig. 21 shows the V_{TH} scaling metrics of 40 nm W_{NW} pFETs and smaller EOT devices have more negative V_{TH}. Similarly, the p-type dopant in AM pFETs would shift V_{TH} positively, which makes the V_{TH} of AM pFETs smaller. Fig. 22 depicts V_{TH} versus W_{NW} of AM pFETs, indicating that smaller W_{NW} increases V_{TH}. Same as nFETs, smaller EOT improves SS significantly for pFETs as shown in Fig. 23. Fig. 24 illustrates the SS dependence on W_{NW} in AM pFETs with an EOT of 2 nm and smaller W_{NW} reduces SS.

Ge Nanowire CMOS:

Because E_F tends to align near the valence band edge in Ge [12] for non-ideal Ge-oxide interface, it's hard to turn ON IM nFETs and turn OFF AM pFETs [9]. Therefore, Ge CMOS with AM nFETs and IM pFETs is preferred. Fig. 25 shows transfer curves of IM pFET and AM nFET inside a 50 nm L_{ch} and 40 nm W_{NW} Ge hybrid CMOS inverter with an EOT of 5 nm. The two devices operate at low drive voltage and show symmetrical performance in terms of V_{TH}, SS, DIBL and I_{ON}, which are crucial for low power and high speed CMOS applications. Fig. 26 presents the output curves of the same nFET and pFET in Fig. 25. The V_{IN}-V_{OUT} curves of this inverter are given in Fig. 27 with voltage gain provided in the inset.

By further reducing the EOT and increasing L_{ch}, much steeper V_{IN}-V_{OUT} curves are achieved, as shown in Fig. 28. Given in the inset, the maximum voltage gain is 54 V/V at a low V_{DD} of 1 V, which approaches the result of the state of the art Si nanowire CMOS inverters [16]. Figs. 29-30 show scaling metrics and W_{NW} dependence of the maximum voltage gain. Related with the output conductance (g_d) in device saturation region, the voltage gain is improved with smaller EOT and W_{NW}. Fig. 31 depicts the maximum voltage gain box plot and histogram based on more than 400 measured inverters with the mean maximum voltage gain of around 15 V/V.

V. Conclusion

We present the first demonstration of Ge nanowire CMOS circuits with H_{NW} of 10 nm, W_{NW} of 40 to 10 nm, L_{ch} of 100 to 40 nm, and EOT of 2 and 5 nm. Various device performance dependences on L_{ch}, W_{NW}, EOT and operation modes are studied in great details. The work demonstrates that Ge with high carrier mobility has the potential for CMOS technology at 7 nm and beyond.

VI. Reference

[1] R. Zhang, et al., *TED*, p.927. 2013. [2] A. Toriumi, et al., *IEDM* 2011, p.646. [3] X. Gong, et al., *IEDM*, 2014, p.231. [4] J. Park, et al., *IEDM* 2008, p.389. [5] J. Mitard, et al., *IEDM* 2008, p.876. [6] R. Pillarisetty, *Nature*, p.324, 2011. [7] H. Wu, et al., *VLSI* 2015, p.58. [8] Y. Kamata, et al., *SSDM* 2014, p.668. [9] J. Mitard, et al., *IEDM*, 2014, p.418. [10] M. van Dal et al., *IEDM*, 2014, p.235 [11] I. Wong, et al., *IEDM*, 2014. p.239. [12] H. Wu, et al., *TED,* p.1419. 2014. [13] R. Rios, et al., *EDL*, p.1170. 2011. [14] R. Kim, et al., *EDL*, p.751, 2015. [15] N. Beppu, et al., IEDM, 2012, p.641. [16] K. Buddharaju, et al., *ESSDRC* 2007, p.303.

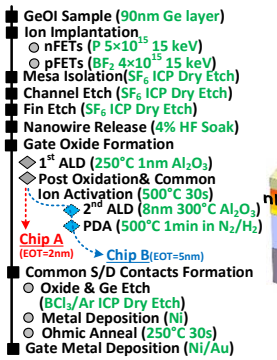

Fig. 1 Fabrication process flow of the Ge nanowire CMOS. Splits on gate oxide are studied.

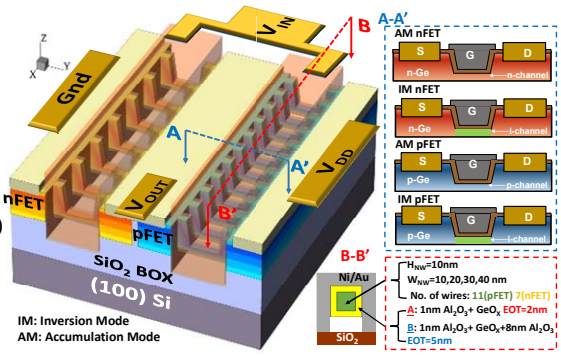

Fig. 2 Device 3D structures and key geometry parameters of the Ge nanowire CMOS. Devices with 4 types of operation modes (AM and IM nFETs, AM and IM pFETs) are listed.

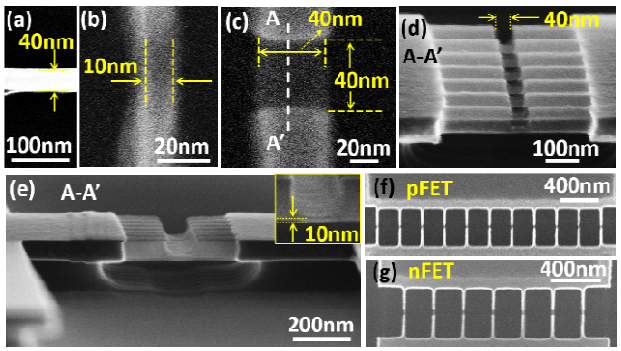

Fig. 3 SEM images of (a) ZEP mask for 40 nm L_{ch} in IM devices. (b) Nanowire with 10 nm W_{NW}. (c) Nanowire with 40 nm W_{NW} and 40 nm L_{ch}. (d) freestanding nanowires with 40 nm L_{ch}. (e) Zoom-out of the Ge nanowires, inset shows the H_{NW} of 10 nm. (f-g) nanowires in p- and nFET.

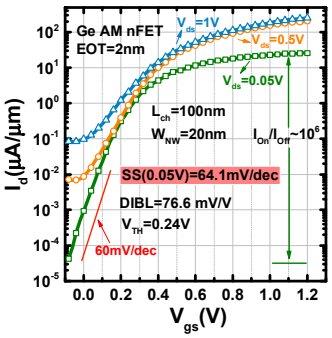

Fig. 4 Transfer curves of a 100 nm L_{ch} and 20 nm W_{NW} Ge AM nanowire nFET with SS=64.1 mV/dec at V_{ds} of 0.05 V. 11 devices have SS < 70 mV/dec.

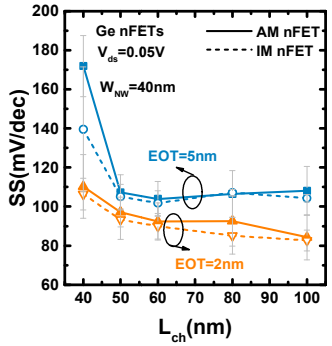

Fig. 5 SS scaling metrics of AM and IM Ge nanowire nFETs with EOT of 2 and 5 nm and W_{NW} of 40 nm. IM and smaller EOT devices have better SS.

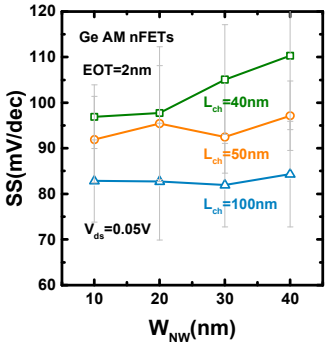

Fig. 6 W_{NW} dependence of the SS of AM Ge nanowire nFETs with an EOT of 2 nm. Smaller W_{NW} devices have better SS.

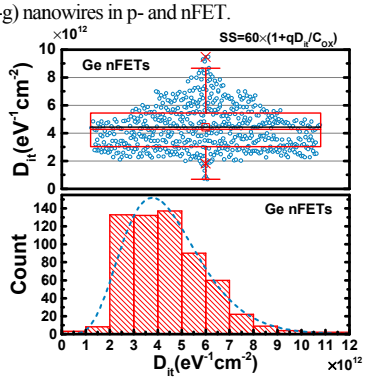

Fig. 7 BOX plot and histogram for mid-gap D_{it} of Ge nanowire nFETs extracted from SS based on more than 800 measured data points.

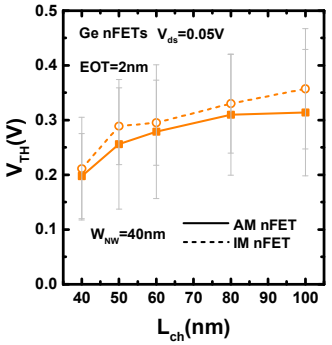

Fig. 8 V_{TH} scaling metrics of Ge nanowire nFETs with an EOT of 2 nm and 40 nm W_{NW}. IM and longer L_{ch} nFETs have larger V_{TH}.

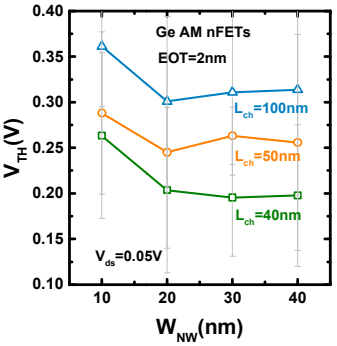

Fig. 9 W_{NW} dependence of the V_{TH} of AM Ge nanowire nFETs with an EOT of 2 nm. Smaller W_{NW} devices have larger V_{TH}.

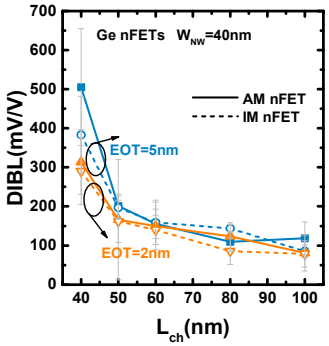

Fig. 10 DIBL scaling metrics of AM and IM Ge nanowire nFETs with an EOT of 2 and 5 nm and W_{NW} of 40 nm. IM and smaller EOT devices have better DIBL.

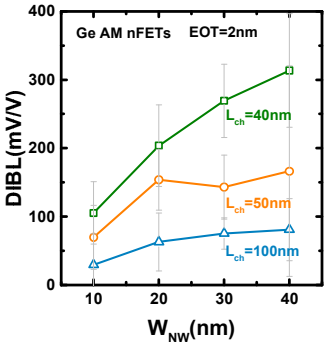

Fig. 11 W_{NW} dependence of the DIBL of AM Ge nanowire nFETs with an EOT of 2 nm. Smaller W_{NW} devices have better DIBL.

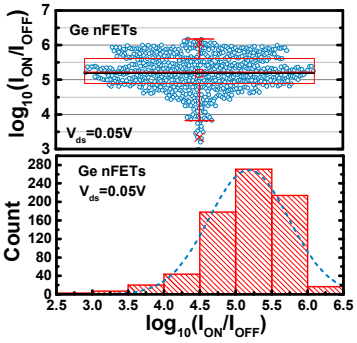

Fig. 12 BOX plot and histogram for the I_{ON}/I_{OFF} of Ge nanowire nFETs at V_{ds} of 0.05 V. based on more than 800 measured data points.

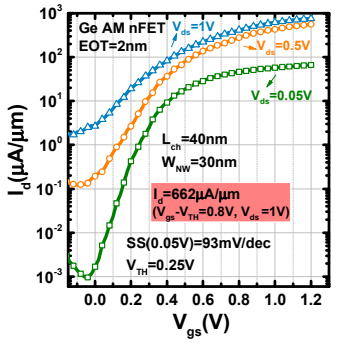

Fig. 13 Transfer curves of a 40 nm L_{ch} and 30 nm W_{NW} Ge AM nanowire nFETs with I_{ON} of 662 μA/μm at V_{ds} of 1 V and V_{gs}-V_{TH} = 0.8 V.

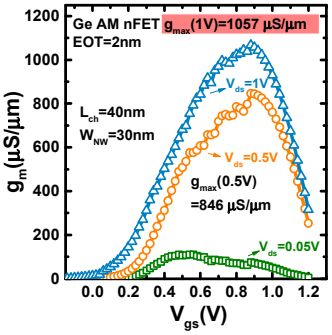

Fig. 14 g_m vs. V_{gs} curves of the same Ge AM nanowire nFETs given in Fig. 13 with 40 nm L_{ch} and 30 nm W_{NW}. Record high g_{max} of 1057 μS/μm is obtained.

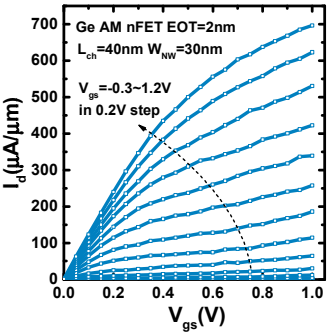

Fig. 15 Output curves of the same Ge AM nanowire nFETs given in Fig. 13 with 40 nm L_{ch} and 30 nm W_{NW}. The I_{max} is around 700 μA/μm.

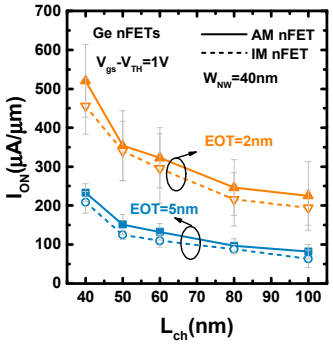

Fig. 16 I_{ON} scaling metrics of AM and IM Ge nanowire nFETs with an EOT of 2 and 5 nm. AM and smaller EOT devices have larger drain current.

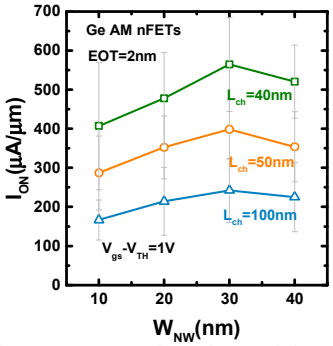

Fig. 17 W_{NW} dependence of the I_{ON} of AM Ge nanowire nFETs with an EOT of 2 nm. The I_{ON} first increases and then decreases with reduced W_{NW}.

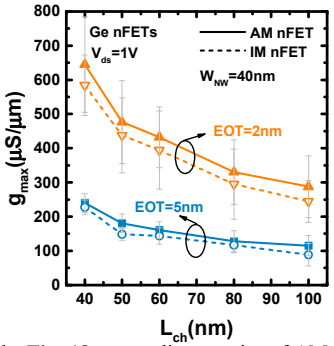

Fig. 18 g_{max} scaling metrics of AM and IM Ge nanowire nFETs with an EOT of 2 and 5 nm. AM and smaller EOT devices have larger trans-conductance.

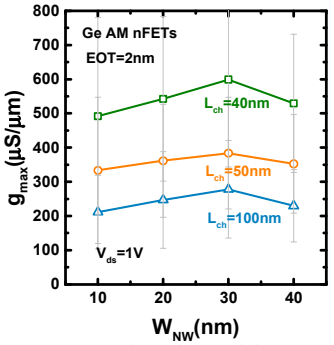

Fig. 19 W_{NW} dependence of the g_{max} of AM Ge nanowire nFETs with an EOT of 2 nm. The g_{max} first increases and then decreases with reduced W_{NW}.

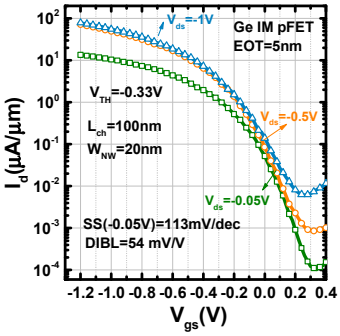

Fig. 20 Transfer curves of a 100 nm L_{ch} and 20 nm W_{NW} Ge IM nanowire pFET with an EOT of 5 nm.

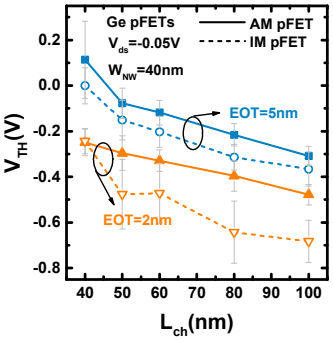

Fig. 21 V_{TH} scaling metrics of AM and IM Ge nanowire pFETs with an EOT of 2 and 5 nm and W_{NW} of 40 nm. IM and thinner EOT pFETs have larger V_{TH}.

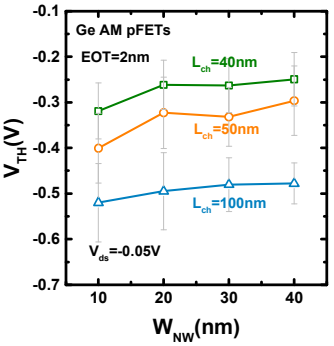

Fig. 22 W_{NW} dependence of the V_{TH} of AM Ge nanowire pFETs with an EOT of 2 nm. Smaller W_{NW} devices have larger V_{TH}.

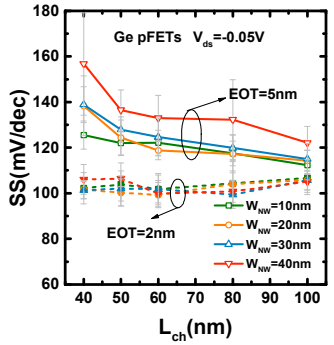

Fig. 23 SS scaling metrics of AM and IM Ge nanowire pFETs with EOT of 2 and 5 nm and W_{NW} of 20, 30, or 40 nm. IM and smaller EOT devices have better SS.

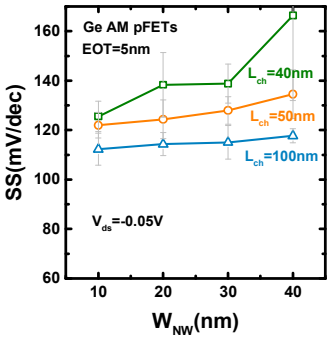

Fig. 24 W_{NW} dependence of the SS of AM Ge nanowire pFETs with EOT of 5 nm. Smaller W_{NW} devices have better SS.

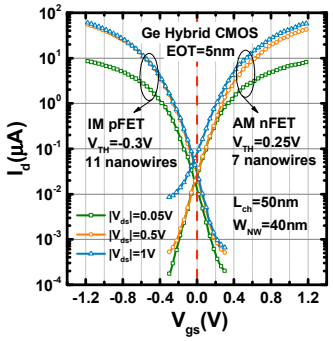

Fig. 25 I_d-V_{gs} of the AM nFET and IM pFET inside a 50 nm L_{ch} and 40 nm W_{NW} hybrid Ge nanowire CMOS inverter with 5 nm EOT. The two show symmetrical performance.

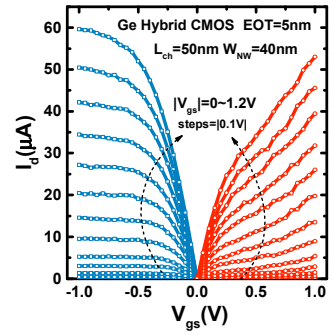

Fig. 26 Output curves of the same AM nFET and IM nFET given in Fig. 25 with $|V_{gs}|$ sweeping from 0 to 1.2 V.

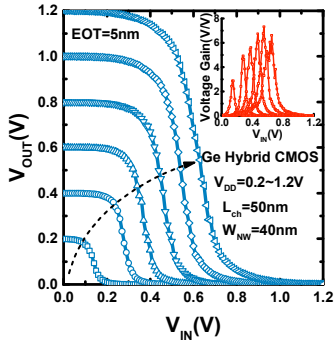

Fig. 27 V_{OUT} versus V_{IN} of the same CMOS inverter shown in Fig. 25. The inset shows the voltage gain.

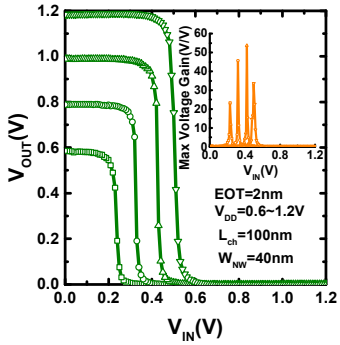

Fig. 28 V_{OUT} versus V_{IN} of a 100 nm L_{ch}, 40 nm W_{NW} and 2 nm EOT Ge nanowire CMOS inverter with highest voltage gain of 54 V/V given in inset.

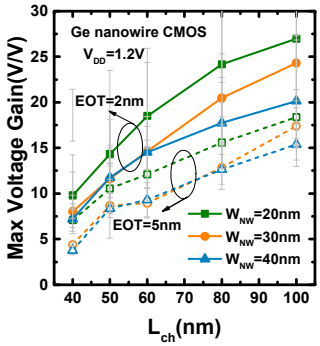

Fig. 29 Maximum voltage gain scaling metrics of Ge nanowire CMOS inverters with an EOT of 2 and 5 nm and W_{NW} of 20, 30 and 40 nm. Thinner EOT devices have larger voltage gain.

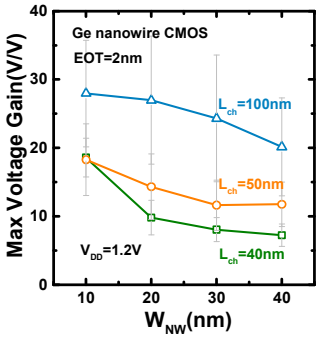

Fig. 30 W_{NW} dependence of the maximum voltage gain of Ge nanowire CMOS inverter with an EOT of 2 nm. Smaller W_{NW} devices have better values.

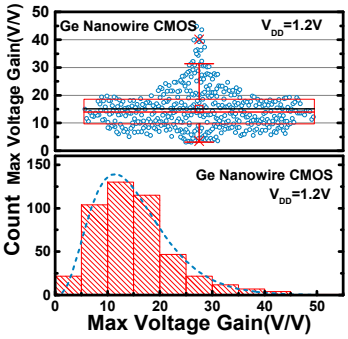

Fig. 31 BOX plot and histogram for the maximum voltage gain of Ge nanowire CMOS inverter at V_{DD} of 1.2 V. based on more than 400 measured devices.