Hysteresis-free Negative Capacitance Germanium CMOS FinFETs with Bi-directional Sub-60 mV/dec

Wonil Chung, Mengwei Si, and Peide D. Ye*
School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA
*Tel: 1-765-494-7611, Fax: 1-765-496-6443, email: yep@purdue.edu

***Abstract*—** In this paper, we report on the first hysteresis-free Ge CMOS FinFETs exhibiting sub-60 mV/dec subthreshold slope (SS) in both forward and reverse sweeps at room temperature. Minimum SS_{rev} of 7 mV/dec and SS_{for} of 17 mV/dec with a large voltage hysteresis of -4.3 V are achieved on 10 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) Ge pFinFET. Ferroelectric (FE) HZO film is integrated with Al_2O_3/GeO_x as a gate stack. Recessed source/drain and fin-channel process scheme is implemented to yield such sub-60 mV/dec 3D devices. With scaled HZO thickness down to 2 nm, Ge pFinFET and nFinFET show SS (forward/reverse) of 56/41 and 43/49 mV/dec respectively. Negligible voltage hysteresis is obtained with -4 mV for pFinFET and 17 mV for nFinFET.

I. Introduction

Power consumption has now become the most serious issue for aggressively scaled CMOS technology. The most effective way to lower the power consumption is to simply reduce the operating voltage of the devices by utilizing low-field high mobility channels and realizing steep slope operations. However, the fundamental limit of 60 mV/dec from Boltzmann distribution of carriers in the conduction band at the source side for a conventional MOSFET limits further operation voltage scaling. With negative capacitance (NC) integrated into the gate stack of a MOS device, SS can be brought below the 60 mV/dec limit while keeping the lateral carrier transport mechanism the same, maintaining high current drivability [1]. NC can be experimentally integrated into the MOS device with FE materials. The most readily-available Si CMOS compatible FE material is $Hf_xZr_{1-x}O_2$ (HZO) [2]. There have been several reported works that show superior switching behavior, both in experiments and simulations, by employing various FE gate stacks on different channel materials [3]–[8]. Germanium has been considered as a promising alternative channel material due to its superior carrier mobility. Multiple high performance Ge devices have been reported so far with various fabrication strategies and structures [9]–[12]. Although various works have been reported on Germanium channel aiming for sub-60mV/dec FETs [13], [14], non-planar Ge n-FinFET with negligible hysteresis and bi-directional SS below 60 mV/dec at room temperature has not been reported. In this work, for the first time, both Germanium n- and p-FinFETs with negligible hysteresis and sub-60mV/dec are reported with scaled FE HZO of 2 nm formed by Atomic Layer Deposition (ALD).

II. Experiments

The key fabrication processes for Ge NC CMOS FinFETs are briefly described in Fig. 1. Germanium on Insulator (GeOI) substrate is used for all device fabrication. Thickness of Ge (100) layer on SiO_2 (400 nm) is 100 nm. After solvent and acid cleaning, n-type (P^+, 5×10^{15} cm^{-2}, 15 keV) and p-type (BF_2^+, $4\times10^{15}cm^{-2}$, 15keV) ion implantation were carried out. Channel recess and fin definition was conducted with SF_6 reactive ion etching (RIE). E-beam lithography was used throughout the whole process to define device features. After definition of fins, gate oxide stack was formed with an initial 1 nm of ALD Al_2O_3 serving as the control layer for post oxidation process through rapid thermal annealing (RTA) at 500 °C in O_2 atmosphere for 30 seconds. The formation of nanometer-thin GeO_x underneath Al_2O_3 significantly improves Ge MOS interface quality [10]. HZO film was deposited with ALD at 250 °C by alternating Hf and Zr precursor pulses. In-situ Al_2O_3 capping was deposited subsequently to prevent the exposure of HZO film to the atmosphere throughout the remaining process steps. The gate stack was annealed in RTA chamber at 500 °C in N_2 for 60 seconds. This process activates the FE property of HZO film which was confirmed from the hysteresis loops in polarization-voltage (P-V) sweeps. S/D area was defined and recess-etched for Ni/n-Ge, Ni/p-Ge contacts [9] and the Ohmic annealing (RTA, 250 °C, N_2, 30s) followed by gate metal deposition was carried out. Fig. 2 and Fig. 3 illustrate the 3D device structures of the fabricated NC FinFET presented in this work. Fig. 3 shows the cross-section view of the oxide gate stack deposited all by ALD. Fig. 4 (a)-(e) show the SEM images of an actual device. Fig. 4(b) and (c) include the images taken before and after defining the fins by dry etching. Multiple fins are clearly found in Fig. 4(e) which shows the side view of the completed device. H_2O was used as oxidant, and TMA, TDMAHf, TDMAZr were used as the precursor sources for Al_2O_3, HfO_2, and ZrO_2, respectively. TDMAT and NH_3 are precursors for metallic TiN.

III. Results and Discussion

ALD HZO film with ALD TiN as top and bottom electrodes was tested and optimized with leakage current measurement (Fig. 5). Breakdown voltage for 10 nm HZO is ±5 V and it decreases with higher annealing temperature due to the crystallization of HZO film. AR-XPS depth profiling measurement was utilized to confirm the atomic % ratio of Hf:Zr:O. With 2 nm of Al_2O_3 protecting the stack's surface, Hf:Zr starts with 1:1 and stays at a slightly increased ratio. Gradually, both Hf (Hf 4f) and Zr (Zr 3d) peaks disappear as the film gets fully-etched revealing substrate peak (Si 2p). The slight increase in Hf:Zr ratio may arise from overlap of O 2s peak (Fig. 7 (a)) near Hf 4f and reduction of HZO due to etching which might act as a source of error in deconvolution process of the Hf 4f peak. As extracted from the top few-nm of HZO where the film is well protected with Al_2O_3 layer, it can be concluded that the film is $Hf_{0.5}Zr_{0.5}O_2$. Fig. 7 (a)

and (b) show the Hf 4f and Zr 3d peak change with increasing etch time. The Fig. 7 (a), (b) also show increase in both metallic Hf and Zr peaks at lower binding energy levels due to oxide reduction caused by sputtering.

Polarization versus electric-field (P-E) measurement using ferroelectric analyzer gives hysteretic P-E graphs shown in Fig. 8 and Fig. 9. They clearly confirm the FE property of the HZO film after 500 °C annealing. Coercive field (E_c) of 1.8 MV/cm and remnant polarization (P_r) of 22 μC/cm^2 can be extracted from Fig. 8 with voltage sweep range of ± 4V. Frequency dependent P-E measurement from the same sample is depicted in Fig. 9(b), showing small frequency dispersion. As expected, as-deposited film shows a linear P-E relation in Fig. 9(a) from which the dielectric constant can be calculated. Capacitance density (μF/cm^2) in Fig. 10 and its inset give the C-E of HZO (10 nm) with and without RTA. From the inset of Fig. 10 with average C/A value of 1.796 μF/cm^2, the dielectric constant of the as-deposited HZO is found to be 20.3. However, after 500 °C RTA, C-E relation shows high spike near the switching voltages (Fig. 10). Such large spikes in capacitance imply sudden significant reduction in EOT or amplification of total capacitance due to NC behavior of HZO film's ferroelectric capacitance (C_{FE}) within that voltage range.

Integrating the FE oxide into MOS device can lead to voltage hysteresis due to hysteretic P-V nature as discussed. Hysteresis-free switching can only be realized if the energy barrier existing in W-shaped energy (U) profile of FE film is carefully compensated with positive capacitance in the device as depicted in Fig. 11 [8], [15]. FE HZO property can be tuned with various parameters such as annealing temperature, atomic ratio of Hf:Zr or the film thickness [2], [8], [16], [17]. Optimization of such properties changes the complex equivalent capacitance network (normal high-k oxide, voltage-dependent C_S, S/D parasitic capacitances and so on) including the negative capacitance of FE HZO. When the network is at appropriate matching condition, negligible hysteresis and sub-60 mV/dec SS can be realized simultaneously [3], [15], [17]. Voltage hysteresis in this paper is defined as, $\Delta V_{T,NMOS} = V_{T,rev} - V_{T,for}$, $\Delta V_{T,PMOS} = V_{T,for} - V_{T,rev}$ and V_T is extracted from 100 nA/μm. According to this definition, ΔV_T is positive if traps dominate and ΔV_T is negative if FE or NC effect dominates (counter clock-wise loop and clock-wise loop for NMOS and PMOS, respectively, for NC effect). All drain currents are normalized by total width of each device (number of fins×[fin width+2×height]).

Fig. 12 presents the transfer characteristics of a Ge pFinFET with 10 nm thick HZO as part of gate stack. Gate voltage is swept in both forward and reverse directions showing bi-directional sub-60 mV/dec SS. To prevent abnormal spikes from point SS extraction, data points were measured every 5 mV or 10 mV steps and then few adjacent data points were linear-fitted for more *conservative* extraction of SS. As observed in Fig. 13, minimum SS for reverse and forward sweeps are 7 and 17 mV/dec respectively. Such abrupt switching accompanies large ΔV_T = -4.3V ($V_{T,for}$ = -1.7 V, $V_{T,rev}$ = 2.6 V) because of the uncompensated C_{FE} and device capacitances [8], [15]. This kind of strong FE-FET behavior might find its potential application as a memory device (FeRAM) which is not the focus of this work for logic device application. Negative differential resistance (NDR) is also observed from reverse-swept output curves (blue and green curves in Fig. 14 (a)) of a Ge pFinFET (L= 260 nm, W= 32 nm, T= 25 nm, $V_{T,for}$ = -2.1 V, $V_{T,rev}$ = 1.8 V). NDR stems from negative DIBL effect as shown in Fig. 14 (c). The negative DIBL effect comes from increased V_{FE} across FE HZO due to drain coupled NC effect, which reduces gate induced charges resulting in lower currents with higher V_D [18]. High voltage hysteresis also causes asymmetric output curves between forward and reverse sweeps as depicted in Fig. 14(a) and (b).

Hysteresis-free NCFET can be realized if NC FE HZO meets appropriate condition with intrinsically positive capacitances presented within the devices [3], [15]. The Ge NC-FETs with 10 nm of FE HZO has a large hysteresis and steep slope of 7 mV/dec which implies too strong NC effect, where C_{FE} is uncompensated by intrinsic device capacitances destabilizing the overall capacitance network. To alleviate the large hysteresis, HZO thickness scaling as thin as 2 nm was implemented for capacitance matching. As a result, hysteresis-free Ge n- and pFinFETs are successfully demonstrated. In Ge nFinFET (Fig. 15 and 16), SS drops to a minimum value of 43 mV/dec at room temperature with 17 mV hysteresis. Positive hysteresis indicates traps dominate, although it is very small and negligible. Similarly, Ge pFinFET (Fig. 17 and 18) demonstrates negligible hysteresis of -4 mV (NC dominates) with minimum SS of 41 mV/dec. Output characteristics in reverse and forward directions are presented in Fig. 19 (a) and (b) respectively to show symmetrical output curves in both voltage sweep directions due to the negligible hysteresis, in great contrast to Fig. 14 (a) and (b). Fig. 20 benchmarks recently reported works which employ HZO for various channel materials with steep slopes.

IV. Conclusion

By integrating FE $Hf_{0.5}Zr_{0.5}O_2$ film into Ge FinFET structures, minimum subthreshold slope of 7 mV/dec is observed. After confirming very strong negative capacitance effect from 10 nm HZO, thinner FE HZO (2 nm) is employed which demonstrate non-hysteretic Ge n- and pFinFET with $|\Delta V_T|$ = 17 and 4 mV, respectively. Bi-directional sub-60mV/dec SS are observed with minimum extracted values of 43 and 41 mV/dec for n- and pFinFET. With optimized FE HZO gate stack, well-behaved 3D Ge CMOS NC-FETs are demonstrated for the first time, which reveal the promise for future low-power integrated circuit applications.

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References

[1] S. Salahuddin et al., *IEDM*, 2008. [2] J. Muller et al., *Nano Lett*., 12, 8, 2012. [3] M. Si et al., *arXiv*:1704.06865, 2017. [4] F. A. McGuire et al., *Nano Lett*., 7b01584, Jul. 2017. [5] M. H. Lee et al., *IEDM*, 2016. [6] G.A. Salvatore et al., *IEDM*, 2008. [7] K. S. Li et al., *IEDM*, 2016. [8] A. I. Khan et al., *IEDM*, 2011. [9] H. Wu et al., *IEDM*, 2015. [10] R. Zhang et al., *EDL*, 37, 7, 2016. [11] C. H. Lee et al., *VLSI*, 2014. [12] M. J. H. van Dal et al., *IEDM*, 2014. [13] C.-J. Su et al., *VLSI*, 2017. [14] J. Zhou et al., *IEDM*, 2016. [15] A. Jain et al., *TED*, 60, 12, 2013. [16] M. H. Park et al., *APL*, 102, 24, 2013. [17] J. Duarte et al., *IEDM*, 2016. [18] G. Pahwa et al., *TED*, 63, 12, 2016.

- **Wafer cleaning, solvent and acid** (GeOI, Ge (100 nm)/SiO_2/Si)
- **Mesa isolation definition** (Dry etching)
- **N-type ion implantation** (**P**, $5x10^{15}$ cm^{-2}, 15 keV)
- **P-type ion implantation** (**BF_2**, $4x10^{15}$ cm^{-2}, 15 keV)
- **Channel recess for Fin height definition** (Dry etching)
- **Fin patterning** (Dry etching)
- **Gate oxide deposition (ALD)**
  - a) **Al_2O_3** 1 nm (250°C)
  - b) Post-oxidation (RTA, O_2, 500°C, 30s)
  - c) **HZO** 2 nm (250°C) or **HZO** 10 nm (250°C)
  - d) **Al_2O_3** Capping, 1 nm (250°C)
- **HZO PDA** (RTA, N_2, 500°C, 60s)
- **Source/Drain recess** (BCl_3 Dry etching)
- **S/D Ni contact deposition**
- **Ohmic anneal** (RTA, N_2, 250°C, 30s)
- **Gate metal, S/D pad definition** (Ni)

Fig. 1. Key fabrication process of Ge NC CMOS FinFETs.

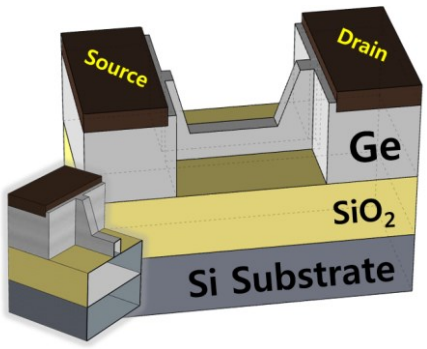

Fig. 2. 3D device structure of a Ge NC FinFET prior to gate metallization.

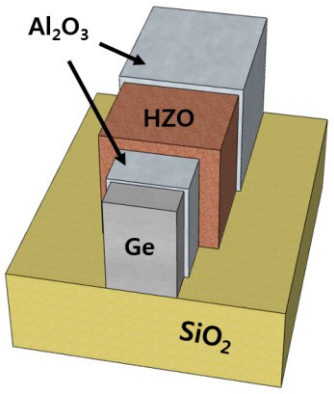

Fig. 3. Gate stack cross-section of a Ge Negative Capacitance FinFET.

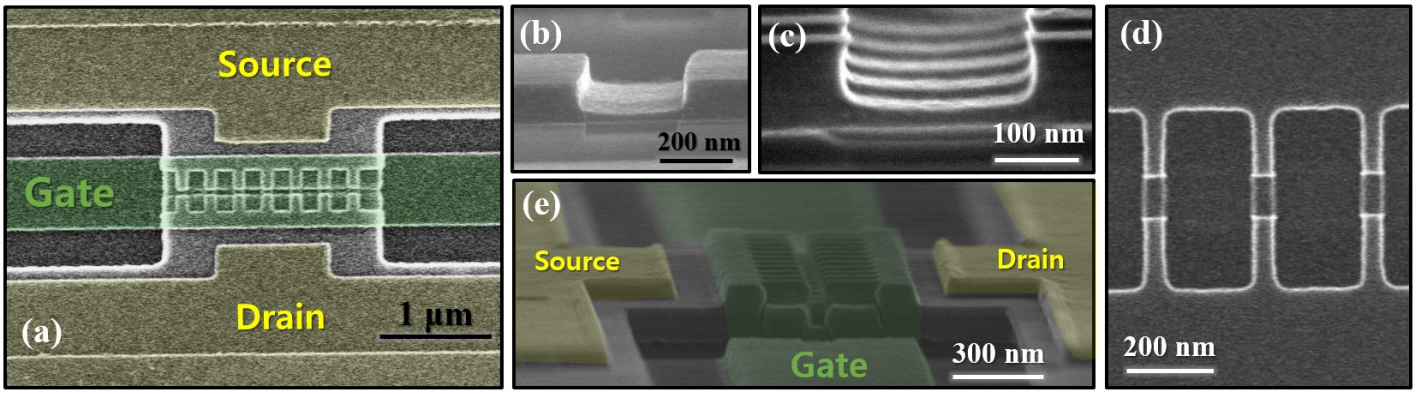

Fig. 4. (a) Top view SEM image of a multiple-FinFET device. (b) Recessed channel with fin height of 21.5nm. (c) Defined fin structure after channel recess. (d) Top view of the defined multiple-Fin structures. (b) ~ (d) are before gate metallization. Side view of (a) is shown in (e).

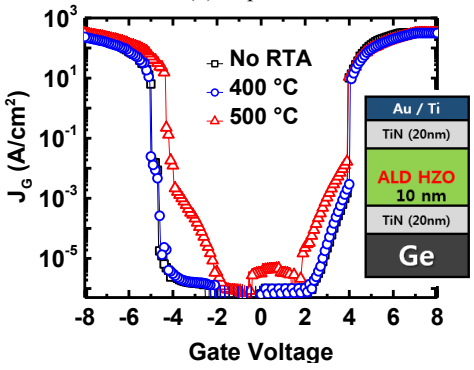

Fig. 5. Leakage current density of a TiN/HZO(10 nm)/TiN capacitor as a function of RTA temperature.

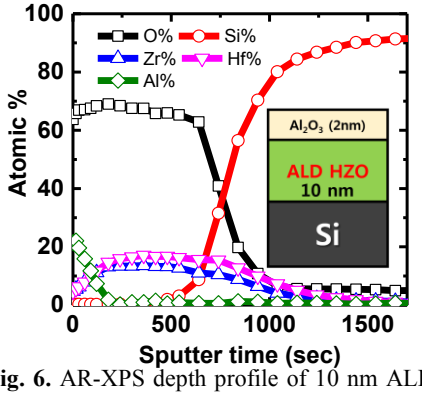

Fig. 6. AR-XPS depth profile of 10 nm ALD HZO film capped with 2 nm Al_2O_3. Atomic % of Hf and Zr is approximately 1:1.

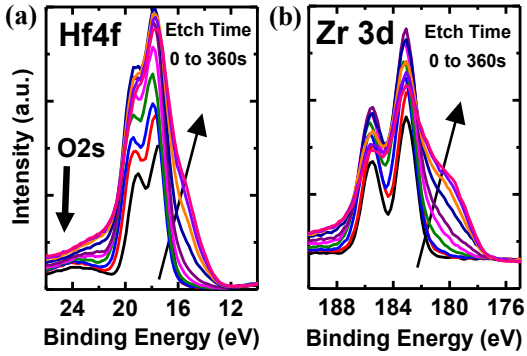

Fig. 7. Etch time dependent XPS (a) Hf 4f and (b) Zr 3d peak show HfO_x and ZrO_x peaks with increasing metallic Hf and Zr with longer etching.

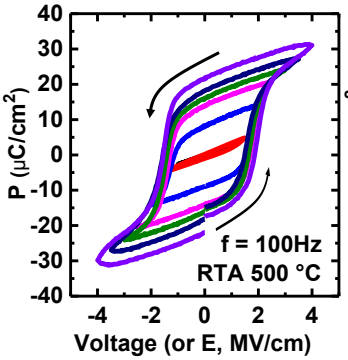

Fig. 8. Measured P-E of 10 nm HZO film (Fig. 5) at different voltage sweep ranges.

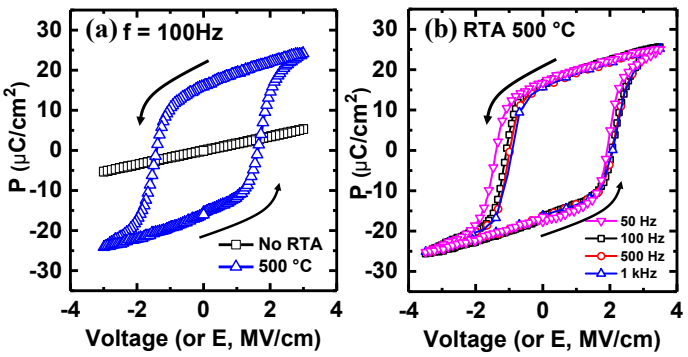

Fig. 9. (a) P-E of the sample in Fig. 5. HZO with RTA (N_2, 500 °C, 60s) shows clear ferroelectric property. (b) Frequency dependent P-E of the sample annealed at 500 °C shows relatively stable behavior within the frequency range.

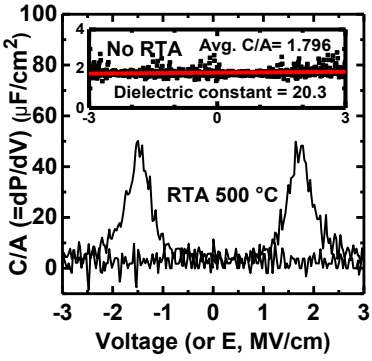

Fig. 10. Capacitance density (C-E) extracted from Fig. 9(a). Inset is the C-E of the sample without RTA showing dielectric property.

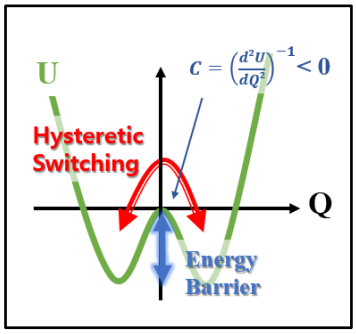

Fig. 11. Conceptual image of origin of voltage hysteresis in a NCFET. Compensation of the energy barrier is needed for hysteresis-free device [15].

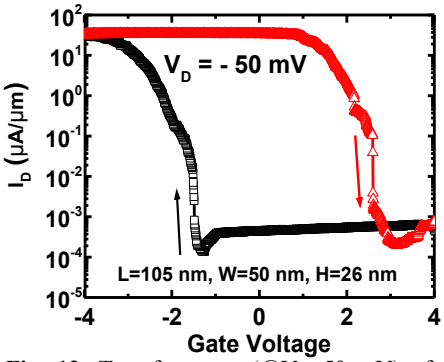

Fig. 12. Transfer curve (@V_D=50 mV) of a Ge pFET (10 nm HZO) showing negative voltage hysteresis with sub-60 mV/dec SS for both sweep directions.

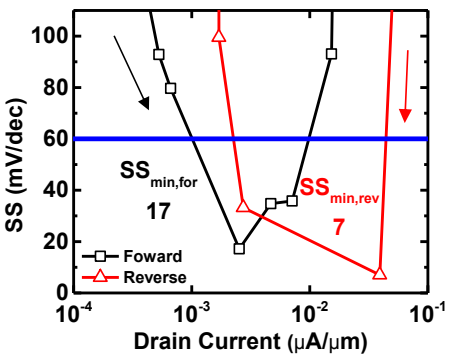

Fig. 13. Extracted sub-threshold slope of device in Fig. 12 shows sub-60 mV/dec in bi-directional sweeps.

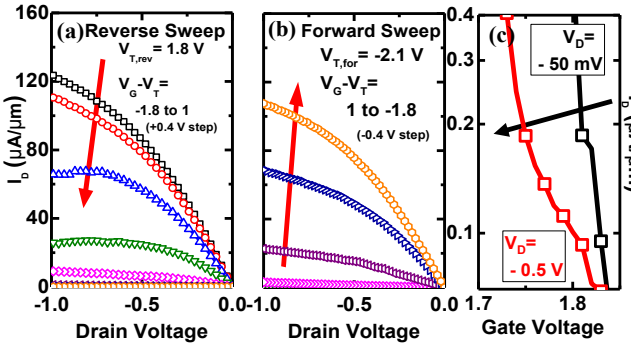

Fig. 14. Output curves with gate voltage swept in (a) forward and (b) reverse direction from a 10 nm HZO pFinFET (L=260 nm). NDR and (c) negative DIBL are observed from the reverse sweep curves.

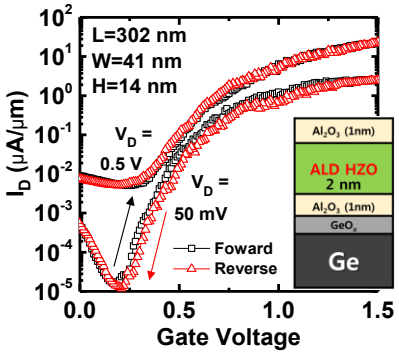

Fig. 15. Hysteresis-free (ΔV_T=17 mV) transfer curves of a Ge nFinFET with 2 nm HZO exhibits sub-60mV/dec SS.

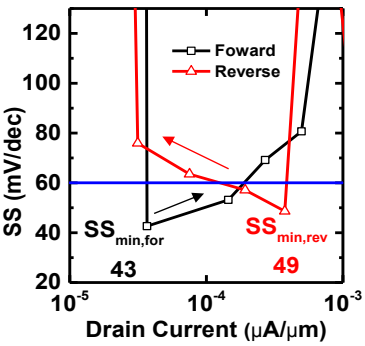

Fig. 16. Subthreshold slope of the device from Fig. 15 reaching down to 43 mV/dec.

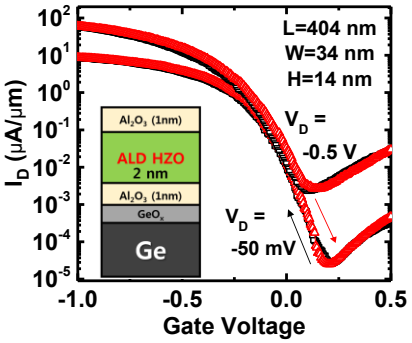

Fig. 17. Hysteresis-free (ΔV_T=-4 mV) transfer curves of a Ge pFinFET with sub-60mV/dec switchings.

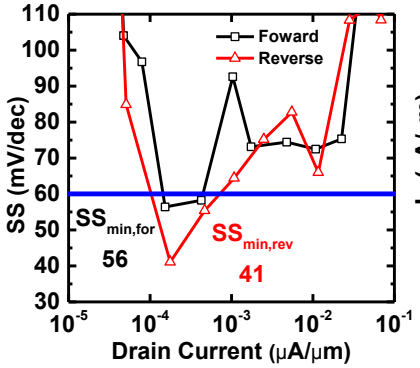

Fig. 18. Extracted sub-threshold slope of the pFinFET also exhibits sub-60mV/dec switchings in both directions.

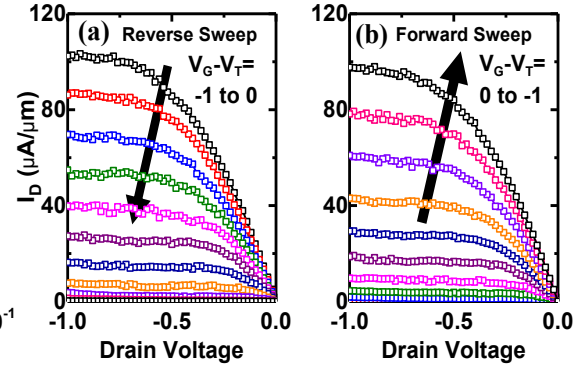

Fig. 19. Unlike 10 nm HZO sample in Fig. 14, both n and p FinFETs with 2 nm HZO gate stack show highly symmetrical output curves due to negligible hysteresis.

	This Work		[14]		[13]		[5]
Material	**GeOI**		Ge Bulk	GeSn	Ge-on-SOI		Si
Gate Stack	**Al_2O_3/$Hf_{0.5}Zr_{0.5}O_2$/Al_2O_3/GeO_x** (a) 10 nm HZO, (b) 2 nm HZO		TaN/$HfZrO_x$ (6.5 nm)/TaN/HfO_2		HZO (7 nm)/GeO_x		TiN/$HfZrO_2$ (1.5nm)/ TiN&TaN/HfO_2
Structure	**pFinFET**	**nFinFET**	Planar pFET	Planar pFET	pFinFET	nFinFET	Planar nFET
W/L (nm)	(a) **50/105** (b) **34/404**	(b) **41/302**	(c) L=5μm (d) L=2μm	(e) L=5μm (f) L=3μm	20/100	20/60	136μm/20μm
Minimum SS	(a) **17(for) / 7(rev)** (b) **56(for) / 41(rev)**	(b) **43(for) / 49(rev)**	(c) 47(for) / 43(rev) (d) 100(for) / 56(rev)	(e) 95(for) / 40(rev) (f) 100 (for/rev)	86 (1way) @300K	75 (1way) @300K	52 (for/rev)
Hysteresis	(a) **-4.3 V** (b) **-4 mV**	(b) **17 mV**	(c) -2.34 V (d) -40 mV	(e) -410 mV (f) -60 mV	34 mV (SS N/A)	N/A	-0.8 mV

Fig. 20. Benchmark of device parameters extracted from various reported experimental steep slope negative capacitance FETs with different structures and channel materials at room temperature. Hysteresis: $\Delta V_{NMOS}=V_{T,rev}-V_{T,for}$ and $\Delta V_{PMOS}=V_{T,for}-V_{T,rev}$.