Carrier Mobility Enhancement by Applying Back-Gate Bias in Ge-on-Insulator MOSFETs

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***Abstract*— In this letter, we comprehensively study the carriers' mobility and the effect of back-gate bias (V_{bg}) in Ge-on-insulator (GeOI) MOSFETs with various working modes, including accumulation mode (AM) nMOSFET, inversion mode (IM) nMOSFET, AM pMOSFET, and IM pMOSFET. The results show that the AM nMOSFETs and pMOSFETs have higher drain currents and carriers' mobility. The electron mobility increases under positive V_{bg} and decreases under negative V_{bg}. While the hole mobility has the opposite V_{bg} dependence. The carriers' mobility of AM MOSFETs is proved to benefit more from V_{bg} due to the increase of carriers' densities. The peak mobility enhancements of more than 100% for holes and 35% for electrons are achieved in GeOI MOSFETs by applying V_{bg}.**

***Index Terms*— Ge-on-insulator, accumulation mode, inversion mode, mobility, back gate bias.**

I. Introduction

THE conventional device scaling down is facing the difficulties associated with MOSFET's performance, including on current, power consumption and short-channel effects [1]–[5]. An effective way to realize high performance and low power consumption MOSFETs is to use the high channel mobility material [5], [6]. Because Ge has high and balanced electron and hole mobility, good compatibility with Si large-scale-integration technologies and good potential of voltage scaling [7]–[9], it is considered as one of the most promising candidates to replace Si. Both Ge nMOSFET and pMOSFET have been intensively studied in the past decade [10]–[13]. High-performance accumulation mode (AM) Ge planar CMOS circuits were realized on Ge-on-insulator (GeOI) substrate [14]. The MOSFET fabricated on GeOI substrate has been regarded as one of the intriguing solutions to improve the electrostatic integrity on Ge [15]–[17]. In addition to its immunity to short channel effects and reduced random dopant fluctuation [18]–[20], using the GeOI substrate with buried oxide structure also enables more efficient threshold voltage (V_{th}) modulation through back-gate bias (V_{bg}) for power/performance optimization [21], [22] and global variability compensation [23]–[26].

Though the AM Ge MOSFETs have been proved to have superior on-state performance compared with the IM MOSFETs [14], the difference in carriers' mobility has not been thoroughly studied. In the meanwhile, the introduced V_{bg} will affect the carriers' density profiles along the channel thickness direction and then also modify the carriers' mobility. Thus the study of the mobility dependence on V_{bg} is of great importance for the understanding and application of V_{bg} in the GeOI MOSFETs.

In this letter, we investigate carriers' mobility in the four types of GeOI MOSFETs, including AM nMOSFET, IM nMOSFET, AM pMOSFET and IM pMOSFET. The carriers' density profiles are studied through TCAD simulation as well as the self-consistent calculation to explain difference in mobility among MOSFETs with different working modes. The effect of V_{bg} on carriers' mobility is also studied in the four types of GeOI MOSFETs. The results show that the AM MOSFET's mobility benefits more from the applied V_{bg}.

II. Experiment

The GeOI substrate is from Soitec, which consists of 90-nm undoped Ge(100) layer, 400-nm buried oxide layer, and a Si(100) substrate. Fig. 1(a) shows the key process of fabrication of the GeOI MOSFETs with recessed channel and source/drain. The pMOSFETs and nMOSFETs were fabricated in parallel for better comparison. A ZEP 520A hard mask was used to define the channel of IM MOSFET. The channel thickness of 40 nm was achieved by controlling the etch time. 1-nm Al_2O_3 capping layer was grown first and then post oxidation was carried out. Afterwards 8-nm Al_2O_3 was deposited. The total equivalent oxide thickness (EOT) is about 5 nm. Ni was deposited as the contact metal in the recessed source/drain region. Finally, gate metal was deposited using Ni/Au. Fig. 1(b) shows the cross section views of AM nMOSFET, IM nMOSFET, AM pMOSFET and IM pMOSFET used in this study. The channel doping concentration is about 5×10^{16} cm^{-3} in the AM MOSFETs. The channel area of the IM devices was covered hard mask during ion implantation, keeping the channel as i-type. Devices with gate length (L_{ch}) of 10 μm and width (W_{ch}) of 100 μm were

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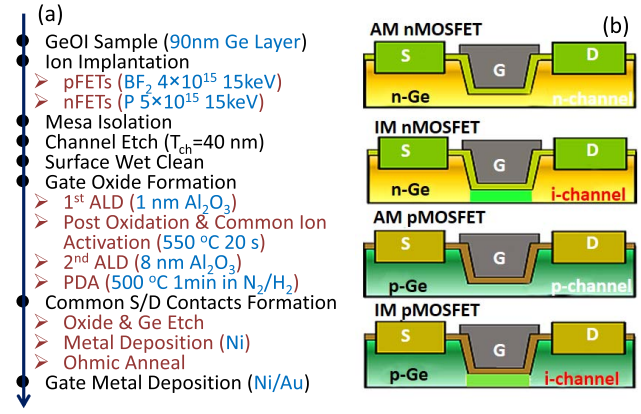

Fig. 1. (a) Key fabrication process of the GeOI MOSFETs with recessed channel and source/drain; (b) Cross section views of devices with four types of operation mode: AM nMOSFET with n-channel, IM nMOSFET with i-channel, AM pMOSFET with p-channel and IM pMOSFET with i-channel.

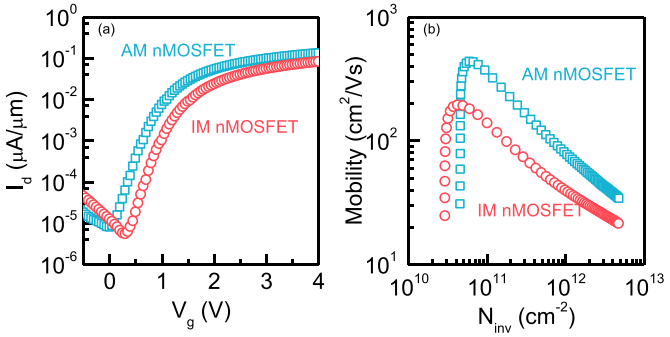

Fig. 2. (a) I_d-V_g curves of AM and IM Ge nMOSFETs with 10 μm L_{ch} and 100 μm W_{ch} at V_{ds} of 0.05 V; (b) Electron mobility versus N_{inv} curves of AM and IM Ge nMOSFETs. AM MOSFET shows better ON-state current and higher electron mobility.

studied to carefully evaluate the carriers' mobility using split-CV method.

III. Results and Discussion

Fig. 2(a) compares the transfer curves of the AM and IM Ge nMOSFETs with the identical device geometry. The AM nMOSFET has a smaller threshold voltage and enhanced drain current (I_d). The phosphorus dopants inside the channel of AM nMOSFET make the device easier to turn on, thus, resulting in a negatively shifted V_{th}. Similar results have been reported in Ge MOSFETs with scaled channel length [14]. The electron mobility was obtained in devices with two different operation modes [Fig. 2(b)]. It is found that the AM nMOSFETs have higher peak and high field mobility. The peak electron mobility of AM nMOSFET is about 400 cm^2/Vs. To further validate the experimental results, TCAD simulation using Sentaurus was executed. Figs. 3(a) and (b) show the simulation results of the electron distribution in AM and IM nMOSFETs. It is clearly shown that AM nMOSFET has more conducting carriers under the same gate overdrive of 1 V, which results in higher I_d in the on-state. Also, considering the quantum confinement in the inversion layer, the envelope function ($\Psi(z)$) and the carrier distribution in the channel depth (z) direction can be calculated by solving the Schrödinger-Poisson equations self-consistently

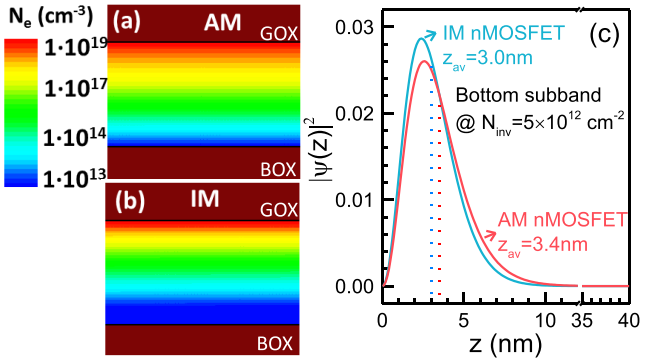

Fig. 3. Simulated on-state (V_g-V_{th} = 1 V) electron distribution inside the channel in (a) AM and (b) IM nMOSFET; (c) self-consistent result of $|\Psi(z)|^2$ versus z in AM and IM nMOSFETs with N_{inv} of 5×10^{12} cm^{-2}. AM nMOSFET has higher electron concentration and larger z_{av}.

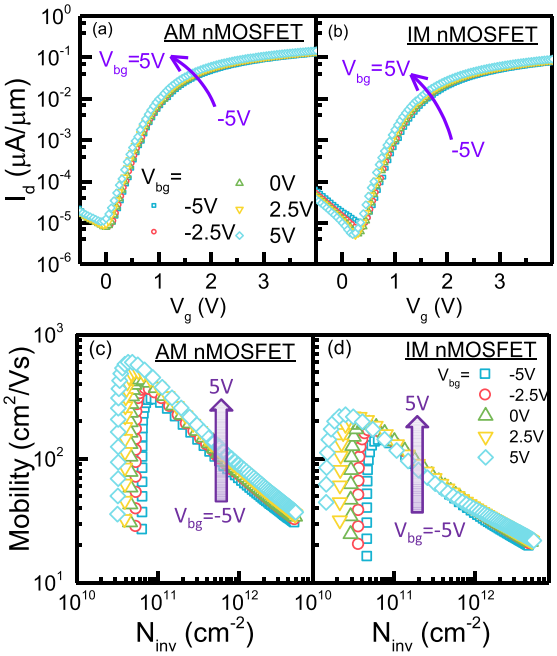

Fig. 4. I_d-V_g curves of (a) AM and (b) IM nMOSFETs under various V_{bg} (from −5 V to 5 V) at V_d of 0.05 V; Electron mobility vs. N_{inv} in (c) AM and (d) IM nMOSFET under various V_{bg} (from −5 V to 5 V). I_d and electron mobility increase under positive V_{bg}.

based on the effective mass approximation [10]. Fig. 3(b) shows the $|\Psi(z)|^2$ versus z in the bottom subband of AM and IM nMOSFETs with the same inversion layer carrier concentration (N_{inv}) of 5×10^{12} cm^{-2}. It is clearly shown that the electrons in AM nMOSFETs populate further away from the interface with an average depth (z_{av}) of 3.4 nm. It is also shown that the electrons in IM nMOSFETs populate closer to the interface (z_{av} = 3 nm) and the carriers are more localized. Thus the surface roughness scattering and phonon scattering would be stronger in the IM nMOSFETs [27]. This is the main reason that IM nMOSFETs have lower peak and high field mobility. The electrons' density distribution also indicates that the front gate control of IM nMOSFET is stronger and it would be less affected by the back gate bias.

Fig. 4 shows the I_d-V_g curves and electron mobility of AM and IM MOSEFTs when being applied back gate biases.

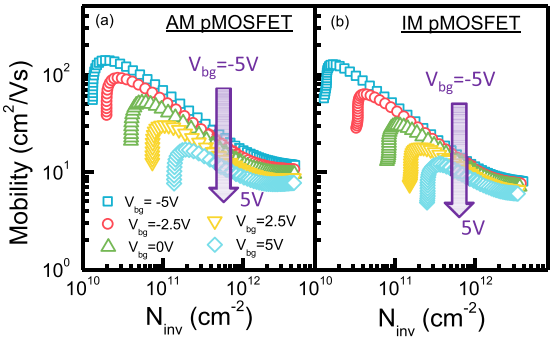

Fig. 5. Hole mobility vs. N_{inv} in (a) AM and (b) IM pMOSFETs under various V_{bg} (from −5 V to 5 V). Hole mobility decreases under positive V_{bg}.

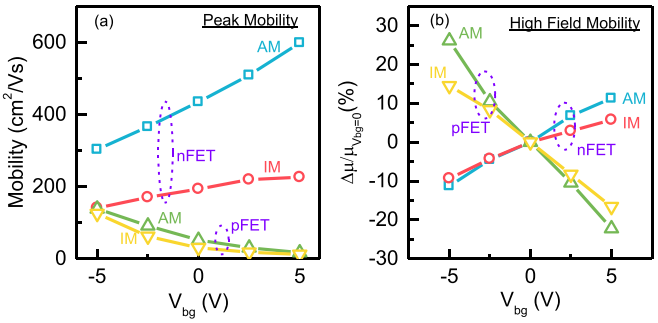

Fig. 6. (a) Peak carrier mobility and (b) the change of high field carrier mobility ($N_{inv} = 5 \times 10^{12}$ cm^{-2} for electron, $N_{inv} = 2 \times 10^{12}$ cm^{-2} for hole) in AM nMOSFET, IM nMOSFET, AM pMOSFET and IM pMOSFET under V_{bg} from −5 V to 5 V.

For both AM and IM nMOSFETs, the V_{th} shifts to negative value when V_{bg} changes from −5 V to 5 V. At the same time, the drain current increases. Considering the electron mobility, both peak mobility and high field mobility decrease under negative V_{bg} and increase under positive V_{bg}. This is because the electrons populate closer to the interface when we applied negative V_{bg}. In this case, there exhibit stronger surface roughness scattering and phonon scattering. The effect of V_{bg} on hole mobility in AM and IM pMOSFETs are studied as well as shown in Fig. 5. In the contrast to nMOSFETs, the peak and high field hole mobility decrease under positive V_{bg} and increase under negative V_{bg}. This is because the holes populate closer to the dielectric interface under positive V_{bg} and further away from the interface under negative V_{bg}.

Fig. 6 illustrates the carriers' peak mobility and the change in high field mobility of all the four types MOSFETs under back gate bias conditions. The AM MOSFETs have higher mobility because of the carriers' broader distributions. The effects of V_{bg} are different in MOSFETs with different operation modes because the front gate control ability is different. The front gate control of IM MOSFETs is stronger and the effect of V_{bg} is smaller. In the contrast, V_{bg} affects more in AM MOSFETs because of the relatively weaker front gate control. In the other words, the AM MOSFETs would benefit more from the V_{bg} in perspective of drain current and mobility. In AM MOSFETs, peak mobility enhancement of more than 100% for holes and 35% for electrons is achieved by applying V_{bg} as demonstrated in these fabricated GeOI MOSFETs.

IV. Conclusion

We have comprehensively studied the carriers' mobility in AM and IM GeOI MOSFETs with and without V_{bg}. It is shown that the AM MOSFETs have higher drain current and carriers' mobility. Electron and hole mobility has the opposite V_{bg} dependence. Electron mobility increases under positive V_{bg} and decreases under negative V_{bg}. The carrier mobility of AM MOSFETs gains significantly under V_{bg} biases.

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References

[1] S. Takagi, R. Zhang, S.-H. Kim, N. Taoka, M. Yokoyama, J.-K. Suh, R. Suzuki, and M. Takenaka, "MOS interface and channel engineering for high-mobility Ge/III-V CMOS," in *IEDM Tech. Dig.*, Dec. 2012, pp. 23.1.1–23.1.4, doi: 10.1109/IEDM.2012.6479085.

[2] R. Pillarisetty, "Academic and industry research progress in germanium nanodevices," *Nature*, vol. 479, pp. 324–328, Nov. 2011, doi: 10.1038/nature10678.

[3] J. A. Del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, pp. 317–323, Nov. 2011, doi: 10.1038/nature10677.

[4] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, vol. 479, pp. 310–316, Nov. 2011, doi: 10.1038/nature10676.

[5] S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, and N. Sugiyama, "Carrier-transport-enhanced channel CMOS for improved power consumption and performance," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 21–39, Jan. 2008, doi: 10.1109/TED.2007.911034.

[6] H. Iwai, "Roadmap for 22 nm and beyond," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1520–1528, 2009, doi: 10.1016/j.mee.2009.03.129.

[7] A. Toriumi, C.-H. Lee, T. Nishimura, S. Wang, K. Kita, and K. Nagashio, "Recent progress of Ge technology for a post-Si CMOS," *ECS Trans.*, vol. 35, no. 3, pp. 443–456, 2011, doi: 10.1149/1.3569936.

[8] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P. A. Pianetta, H.-S. P. Wong, and S. C. Krishna, "High-mobility Ge N-MOSFETs and mobility degradation mechanisms," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 59–66, Jan. 2011, doi: 10.1109/TED.2010.2088124.

[9] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, "High-mobility Ge pMOSFET with 1-nm EOT Al_2O_3/GeO_x/Ge gate stack fabricated by plasma post oxidation," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 335–341, Feb. 2012, doi: 10.1109/TED.2011.2176495.

[10] W. Wu, X. Li, J. Sun, R. Zhang, Y. Shi, and Y. Zhao, "Comparison of different scattering mechanisms in the Ge (111), (110), and (100) inversion layers of nMOSFETs with Si nMOSFETs under high normal electric fields," *IEEE Trans. Electron Devices*, vol. 62, no. 4, pp. 1136–1142, Apr. 2015, doi: 10.1109/TED.2015.2398733.

[11] J. Mitard, B. De Jaeger, F. E. Leys, G. Hellings, K. Martens, G. Eneman, D. P. Brunco, R. Loo, J. C. Lin, D. Shamiryan, T. Vandeweyer, G. Winderickx, E. Vrancken, C. H. Yu, K. De Meyer, M. Caymax, L. Pantisano, M. Meuris, and M. M. Heyns, "Record I_{ON}/I_{OFF} performance for 65 nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability," in *IEDM Tech. Dig.*, Dec. 2008, pp. 873–876, doi: 10.1109/IEDM.2008.4796837.

[12] R. Zhang, J.-C. Lin, X. Yu, M. Takenaka, and S. Takagi, "Examination of physical origins limiting effective mobility of Ge MOSFETs and the improvement by atomic deuterium annealing," in *Proc. Symp. VLSI Technol.*, Jun. 2013, pp. T26–T27.

[13] C. Lee, C. Lu, T. Tabata, T. Nishimura, K. Nagashio, and A. Toriumi, "Enhancement of high-N_S electron mobility in sub-nm EOT Ge n-MOSFETs," in *Proc. Symp. VLSI Technol.*, Jun. 2013, pp. T28–T29.

[14] H. Wu, N. Conrad, W. Luo, and P. D. Ye, "First experimental demonstration of Ge CMOS circuits," in *IEDM Tech. Dig.*, Dec. 2014, pp. 9.3.1–9.3.4, doi: 10.1109/IEDM.2014.7047016.

[15] E. Pop, C. O. Chui, R. Dutton, S. Sinha, and K. Goodson, "Electro-thermal comparison and performance optimization of thin-body SOI and GOI MOSFETs," in *IEDM Tech. Dig.*, Dec. 2004, pp. 411–414, doi: 10.1109/IEDM.2004.1419172.

[16] S. W. Bedell, A. Majumdar, J. A. Ott, J. Arnold, K. Fogel, S. J. Koester, and D. K. Sadana, "Mobility scaling in short-channel length strained Ge-on-insulator P-MOSFETs," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 811–813, Jul. 2008, doi: 10.1109/LED.2008.2000713.

[17] T. Maeda, K. Ikeda, S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, "High mobility Ge-on-insulator p-channel MOSFETs using Pt germanide Schottky source/drain," *IEEE Electron Device Lett.*, vol. 26, no. 2, pp. 102–104, Feb. 2005, doi: 10.1109/LED.2004.841442.

[18] Q. Liu, A. Yagishita, N. Loubet, A. Khakifirooz, P. Kulkarni, T. Yamamoto, K. Cheng, M. Fujiwara, J. Cai, D. Dorman, S. Mehta, P. Khare, K. Yako, Y. Zhu, S. Mignot, S. Kanakasabapathy, S. Monfray, F. Boeuf, C. Koburger, H. Sunamura, S. Ponoth, A. Reznicek, B. Haran, A. Upham, R. Johnson, L. F. Edge, J. Kuss, T. Levin, N. Berliner, E. Leobandung, T. Skotnicki, M. Hane, H. Bu, K. Ishimaru, W. Kleemeier, M. Takayanagi, B. Doris, and R. Sampson, "Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22 nm node and beyond," in *Proc. Symp. VLSI Technol.*, Jun. 2010, pp. 61–62, doi: 10.1109/VLSIT.2010.5556120.

[19] O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelle, B.-Y. Nguyen, and S. Deleonibus, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4, doi: 10.1109/IEDM.2008.4796663.

[20] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi, L. F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet, S. Holmes, S. Mehta, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, B. S. Haran, Z. Zhu, L. H. Vanamurth, S. Fan, D. Horak, H. Bu, P. J. Oldiges, D. K. Sadana, P. Kozlowski, D. McHerron, J. O'Neill, and B. Doris, "Extremely thin SOI (ETSOI) CMOS with record low variability for low power system-on-chip applications," in *IEDM Tech. Dig.*, Dec. 2009, pp. 1–4, doi: 10.1109/IEDM.2009.5424422.

[21] F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J.-P. Noel, C. Fenouillet-Béranger, J.-P. Mazellier, P. Perreau, T. Poiroux, Y. Morand, T. Morel, S. Allegret, V. Loup, S. Barnola, F. Martin, J.-F. Damlencourt, I. Servin, M. Cassé, X. Garros, O. Rozeau, M.-A. Jaud, G. Cibrario, J. Cluzel, A. Toffoli, F. Allain, R. Kies, D. Lafond, V. Delaye, C. Tabone, L. Tosti, L. Brévard, P. Gaud, V. Paruchuri, K. K. Bourdelle, W. Schwarzenbach, O. Bonnin, B.-Y. Nguyen, B. Doris, F. Boeuf, T. Skotnicki, and O. Faynot, "Low leakage and low variability ultra-thin body and buried oxide (UT2B) SOI technology for 20 nm low power CMOS and beyond," in *Proc. Symp. VLSI Technol.*, Jun. 2010, pp. 57–58, doi: 10.1109/VLSIT.2010.5556122.

[22] C. Fenouillet-Beranger, O. Thomas, P. Perreau, J.-P. Noel, A. Bajolet, S. Haendler, L. Tosti, S. Barnola, R. Beneyton, C. Perrot, C. de Buttet, F. Abbate, F. Baron, B. Pernet, Y. Campidelli, L. Pinzelli, P. Gouraud, M. Cassé, C. Borowiak, O. Weber, F. Andrieu, K. K. Bourdelle, B. Y. Nguyen, F. Boedt, S. Denorme, F. Boeuf, O. Faynot, and T. Skotnicki, "Efficient multi-VT FDSOI technology with UTBOX for low power circuit design," in *Proc. Symp. VLSI Technol.*, Jun. 2010, pp. 65–66, doi: 10.1109/VLSIT.2010.5556118.

[23] J. W. Tschanz, J. T. Kao, S. G. Narendra, R. Nair, D. A. Antoniadis, A. P. Chandrakasan, and V. De, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1396–1402, Nov. 2002, doi: 10.1109/JSSC.2002.803949.

[24] S. Narendra, D. Antoniadis, and V. De, "Impact of using adaptive body bias to compensate die-to-die Vt variation on within-die Vt variation," in *Proc. Int. Symp. Low Power Electron. Design*, 1999, pp. 229–232, doi: 10.1145/313817.313932.

[25] Y. Yasuda, Y. Akiyama, Y. Yamagata, Y. Goto, and K. Imai, "Design methodology of body-biasing scheme for low power system LSI with multi-V_{th} transistors," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 2946–2952, Nov. 2007, doi: 10.1109/TED.2007.906964.

[26] H. Mostafa, M. Anis, and M. Elmasry, "Adaptive body bias for reducing the impacts of NBTI and process variations on 6T SRAM cells," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 12, pp. 2859–2871, Dec. 2011, doi: 10.1109/TCSI.2011.2158708.

[27] S.-I. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I-Effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2357–2362, Dec. 1994, doi: 10.1109/16.337449.