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## Inversion-mode GaAs wave-shaped field-effect transistor on GaAs (100) substrate

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Inversion-mode GaAs wave-shaped metal-oxide-semiconductor field-effect transistors (WaveFETs) are demonstrated using atomic-layer epitaxy of  $\text{La}_2\text{O}_3$  as gate dielectric on (111)A nano-facets formed on a GaAs (100) substrate. The wave-shaped nano-facets, which are desirable for the device on-state and off-state performance, are realized by lithographic patterning and anisotropic wet etching with optimized geometry. A well-behaved  $1\ \mu\text{m}$  gate length GaAs WaveFET shows a maximum drain current of  $64\ \text{mA}/\text{mm}$ , a subthreshold swing of  $135\ \text{mV}/\text{dec}$ , and an  $I_{\text{ON}}/I_{\text{OFF}}$  ratio of greater than  $10^7$ . © 2015 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4913431>]

GaAs has been considered to replace Si in logic applications for decades due to its high electron mobility.<sup>1</sup> To achieve high on-current surface-channel inversion-mode n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) on GaAs (100) substrate is a long-time challenge. The main obstacle is the lack of high-quality, thermodynamically stable dielectric on GaAs that can match the device criteria as  $\text{SiO}_2$  on Si such as a mid-gap interface trap density ( $D_{\text{it}}$ ) around  $10^{10}\ \text{cm}^{-2}\ \text{eV}^{-1}$ . During the past decades, tremendous efforts have been made to improve the oxide/GaAs interface with most of focus on different types of oxides and formation methods.<sup>2–10</sup> Recent work finds that the oxide/GaAs interface quality is strongly dependent on semiconductor surface orientations. GaAs MOSFETs fabricated on (111)A surface exhibit much higher on-state current ( $I_{\text{ON}}$ ) than other surface-orientations such as (100) and (111)B even with the same atomic-layer-deposited (ALD) oxide.<sup>11</sup> More interestingly, much larger  $I_{\text{ON}}$  can be achieved on GaAs (111)A substrate with single crystalline La-based oxide dielectrics by atomic-layer-epitaxy (ALE).<sup>12</sup> Mid-gap  $D_{\text{it}}$  or Fermi-level-pinning problem is significantly reduced with epitaxial  $\text{La}_2\text{O}_3$  on GaAs (111)A surface,<sup>13,14</sup> because the number of dangling bonds are dramatically reduced due to the nature of epitaxial oxide/semiconductor interface. However, GaAs (111)A substrate is technologically less important than the widely available GaAs (100) substrate, in particular, for the development of a manufacturable device technology.

In this letter, we demonstrate GaAs wave-shaped MOSFETs (WaveFETs) on a GaAs (100) substrate by nano-engineering to form ALE  $\text{La}_2\text{O}_3$  on (111)A nano-facets. GaAs (111)A surface is achieved on a GaAs (100) substrate by the development of a well-controlled anisotropic wet etching process. GaAs MOSFETs are formed on wave-shaped (111)A surface channels with epitaxial  $\text{La}_2\text{O}_3$  as

dielectric. But, all devices are fabricated on GaAs (100) substrates. These devices have on-state current ( $I_{\text{ON}}$ ) of  $64\ \text{mA}/\text{mm}$  and transconductance ( $g_m$ ) of  $32\ \text{mS}/\text{mm}$  with sub-threshold swing (SS) around  $135\ \text{mV}/\text{dec}$ . This work opens a route to realize high-performance GaAs MOSFETs on (100) substrates potentially. The process development and deep understanding of surface chemistry on these nano-facets could also be very important for the emerging 3D III–V devices.<sup>15–23</sup>

Figures 1(a) and 1(b) show the schematic view and cross-sectional view of a GaAs WaveFET in this work fabricated on a semi-insulating GaAs (100) substrate with an ALE high-k dielectric. The detailed process flow is described following. An HF and  $\text{H}_2\text{O}_2$  based anisotropic wet etching process<sup>24</sup> was applied to form the wave structure with Ti/Au as hard mask illustrated in Figure 2. MOSFET fabrication starts with 2-in. semi-insulating GaAs (100) substrates. As-received wafers were first degreased at room temperature by acetone for 10 min, methanol for 5 min, and isopropanol

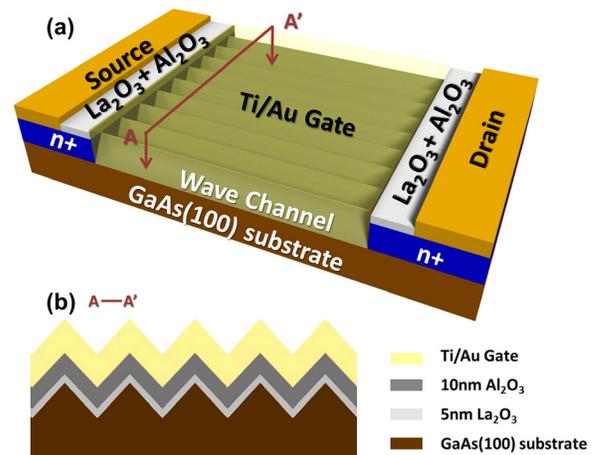


FIG. 1. (a) Schematic and (b) Cross-sectional view of an inversion-mode GaAs (100) WaveFET with ALE  $\text{La}_2\text{O}_3$ .

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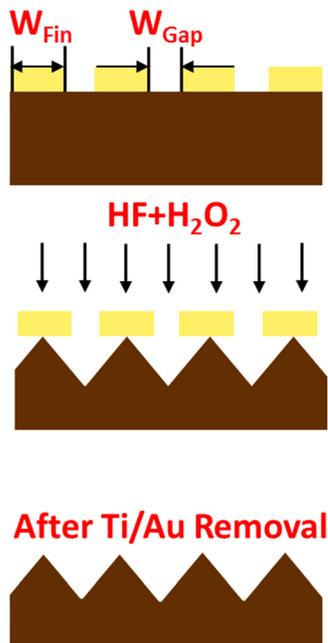


FIG. 2. Illustration of wave channel formation by anisotropic wet etching. GaAs (111)A surface on these nano-facets is achieved by anisotropic wet etching of GaAs using HF solution.

for 5 min, respectively. The wave patterns were defined by electron beam lithography and Ti/Au (2 nm/10 nm) were deposited by electron beam evaporation. After lift-off process, periodically patterned Ti/Au strip hard masks were formed as illustrated in Figure 2. Then, the wafers were dipped into HF (49%): H<sub>2</sub>O<sub>2</sub> (30%) (10:129) based solution to form the wave-shaped channels for 3 s. The wet etching time depends on the design of the fin-width ( $W_{\text{Fin}}$ ) and the gap-width ( $W_{\text{Gap}}$ ) as depicted in Figure 2.  $W_{\text{Fin}}$ ,  $W_{\text{Gap}}$ , and etching time were optimized to achieve the maximum effective length width. The (111)A surface was obtained due to the anisotropic property of the wet etching process.<sup>25</sup> The realization of (111)A other than (111)B is further confirmed by the electrical properties of the fabricated devices since the Fermi level on (111)B is expected to be pinned.<sup>11</sup> After removal of Ti/Au hard mask by KI solution, the wafers were dipped into buffered oxide etch (BOE) for 30 s and then soaked in 10% (NH<sub>4</sub>)<sub>2</sub>S for 15 min for surface passivation. After deionized water rinse, the wafers were quickly transferred into ALD deposition chamber. 5 nm epitaxial La<sub>2</sub>O<sub>3</sub> and 10 nm amorphous Al<sub>2</sub>O<sub>3</sub> were then deposited by ALE/ALD. GaAs WaveFETs with 8 nm amorphous Al<sub>2</sub>O<sub>3</sub> only as gate dielectric were also fabricated as the control sample. The epitaxial La<sub>2</sub>O<sub>3</sub> thin films employed here were deposited from the precursors lanthanum tris(N,N'-diisopropylformamidate) and H<sub>2</sub>O at 385 °C, while the amorphous Al<sub>2</sub>O<sub>3</sub> oxide capping layer was deposited with precursors of trimethylaluminum (TMA) and H<sub>2</sub>O at 300 °C. The precursor and pulse time was all 1 s. The purpose of Al<sub>2</sub>O<sub>3</sub> capping layer is to prevent the reaction between La<sub>2</sub>O<sub>3</sub> and moisture in air and water during the process. Source and drain (S/D) regions were formed by a two-step Si implantation with dose of  $1 \times 10^{14} \text{ cm}^{-2}$  at 30 keV and  $1 \times 10^{14} \text{ cm}^{-2}$  at 80 keV, followed by an 850 °C rapid thermal annealing (RTA) in N<sub>2</sub> for 15 s. S/D ohmic contact area was first defined by

electron-beam lithography, and then BCl<sub>3</sub>/Ar inductively coupled plasma (ICP) dry etching was applied to remove the Al<sub>2</sub>O<sub>3</sub> and HCl wet etching was applied to remove the La<sub>2</sub>O<sub>3</sub> above metal contact area. Au/Ge/Au/Ni/Au (5 nm/12.5 nm/15 nm/9 nm/50 nm) contact was then formed followed by a 420 °C RTA in N<sub>2</sub> for 15 s. Then, Ti/Au (30 nm/60 nm) were deposited as gate electrodes and test pads. All patterns were defined by a Vistec VB-6 UHR electron beam lithography system. The fabricated devices have gate lengths ( $L_g$ ) of 1 μm, 2 μm, and 4 μm.

The illustration of anisotropic wet etch process (HF and H<sub>2</sub>O<sub>2</sub>) is shown in Fig. 3. In this process, the wave patterned direction is critical. The wave structure has to be patterned along (01 $\bar{1}$ ) other than (011) as shown in Figure 3(a). The effect of wave pattern direction is shown by cross-sectional scanning electron microscopy (SEM) pictures in Figures 3(b) and 3(c). Hard mask strips were patterned along (01 $\bar{1}$ ) in Figure 3(b) and along (011) in Figure 3(c). Clear (111) surface is shown in Figure 3(b), but irregular structures are formed if hard mask strips were patterned along (011). Meanwhile, optimized  $W_{\text{Fin}}$  and  $W_{\text{Gap}}$  are also important to form compact wave structure with sharp corners, so that the maximum channel width with (111)A surface can be realized within the fixed channel pitch from the top. Figure 4(a) shows the transmission electron microscopy (TEM) picture of the cross section of the wave channel. A high-resolution TEM image of the epitaxial interface, taken from a sample with 5 nm La<sub>2</sub>O<sub>3</sub>/10 nm Al<sub>2</sub>O<sub>3</sub> as gate dielectric, is also shown in Figure 4(b). The lattice mismatch of La<sub>2</sub>O<sub>3</sub> on GaAs (111)A is ~0.04%. It is evident from TEM image that a flat and sharp interface is formed even on fabricated (111)A nano-facet. It has been proved by C-V measurement that the epitaxial La<sub>2</sub>O<sub>3</sub>/GaAs (111)A interface exhibits  $D_{\text{it}}$  on the order of  $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , which is far below the  $D_{\text{it}}$  level of traditional amorphous oxide on GaAs (111)A surface.<sup>12,13</sup> Figure 4(c) depicts the top view SEM image of one finished GaAs WaveFET with a gate length of 2 μm.

Well-behaved output, transfer, and trans-conductance characteristics of a 1 μm-gate-length inversion-mode GaAs WaveFET are plotted in Figure 5, showing a maximum drain current ( $I_{\text{D,max}}$ ) of 64 mA/mm at a gate bias ( $V_{\text{GS}}$ ) of 4 V and a drain bias ( $V_{\text{DS}}$ ) of 2 V, a maximum  $g_m$  of 32 mS/mm at  $V_{\text{DS}} = 2 \text{ V}$ , and threshold voltage ( $V_{\text{T}}$ ) of 1.32 V. SS of

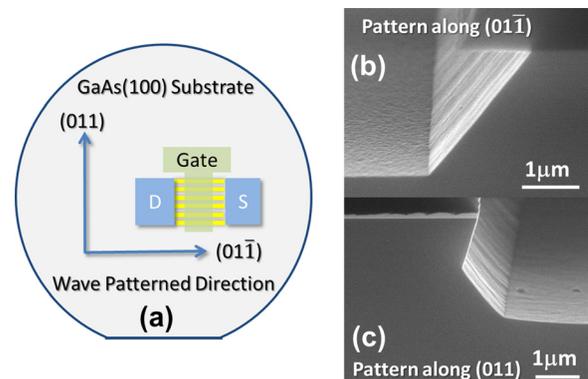


FIG. 3. (a) Schematic diagram of wave patterned orientation. (b) and (c) Cross-sectional SEM images of wave structures patterning along (01 $\bar{1}$ ) and (011) orientations.

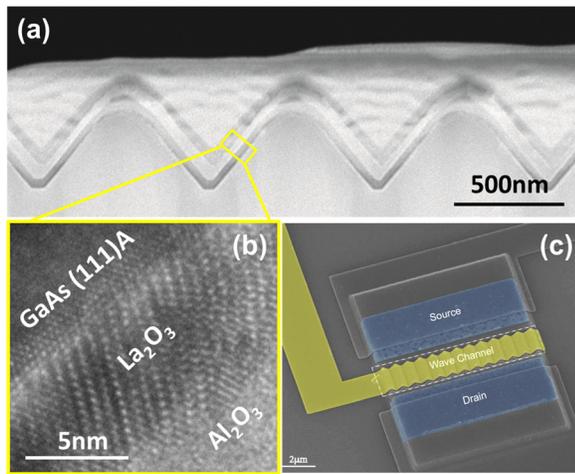


FIG. 4. (a) Cross-sectional STEM image of GaAs WaveFET structure covered with  $\text{La}_2\text{O}_3$  and  $\text{Al}_2\text{O}_3$ . (b) HRTEM image of  $\text{La}_2\text{O}_3/\text{GaAs}$  interface. Epitaxial  $\text{La}_2\text{O}_3$  forms a flat and sharp interface on wave surface. (c) SEM image of a GaAs (100) WaveFET device top view with  $L_g = 2 \mu\text{m}$ . Parallel wave structures are clearly shown as device channel.

$\sim 135 \text{ mV/dec}$  is obtained with an equivalent oxide thickness (EOT) of  $\sim 6 \text{ nm}$ , indicating a mid-gap interface trap density of  $4.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ , which is simply estimated from equation  $SS \sim 60 \times (1 + qD_{it}/C_{ox}) \text{ mV/dec}$ . SS could be further improved by optimizing fabrication process and reducing EOT. It will also improve the extrinsic drain current and trans-conductance by reducing the EOT of the dielectric and improving interface quality. Devices with different gate length  $L_g$  (1, 2 and  $4 \mu\text{m}$ ) show similar SS and  $V_T$  (not

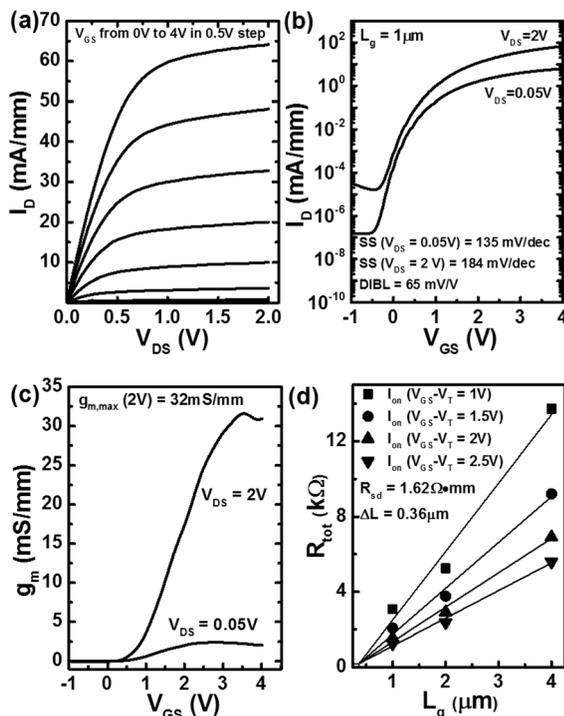


FIG. 5. (a) Output and (b) transfer (c)  $g_m$  characteristics of a GaAs WaveFET with  $L_g = 1 \mu\text{m}$ . The device shows maximum drain current of  $64 \text{ mA/mm}$ , a subthreshold swing of  $135 \text{ mV/dec}$ , a peak trans-conductance of  $32 \text{ mS/mm}$ , and an  $I_{ON}/I_{OFF}$  greater than  $10^7$ . (d) Measured total resistance versus different mask gate lengths as a function of gate bias.  $R_{SD}$  of  $1.62 \Omega\text{-mm}$  and  $\Delta L$  of  $\sim 0.36 \mu\text{m}$  are determined from the fitting lines.

shown), indicating that these devices are weakly affected by short channel effects. It is also expected that these GaAs devices with a large bandgap and 3D wave structures must have better immunity to short channel effects. The GaAs WaveFET with epitaxial  $\text{La}_2\text{O}_3$  demonstrated here has  $I_{D,max}$  about  $1000 \times$  larger than that of the reference GaAs sample with amorphous  $\text{Al}_2\text{O}_3$  dielectric (not shown) and about  $10000 \times$  larger than that of GaAs planar MOSFET on GaAs (100) substrate with amorphous  $\text{Al}_2\text{O}_3$ .<sup>11</sup> GaAs planar MOSFETs on GaAs (100) substrate with  $\text{La}_2\text{O}_3$  as gate dielectric were also fabricated. Without the special surface orientation to form (111) hexagonal template, poor quality  $\text{La}_2\text{O}_3$  dielectric was formed on GaAs (100) surface showing a weak gate modulation and minuscule  $I_{D,max}$ . Figure 5(d) summarizes the effective gate length  $L_{eff}$  and the series resistance ( $R_{SD}$ ) extracted by plotting  $R_{tot}$  versus  $L_g$ , where  $R_{tot}$  represents the total channel resistance measured from devices with various gate lengths under  $V_{GS} - V_T$  from 1 to  $2.5 \text{ V}$ .  $R_{SD}$  is determined to be  $1.62 \Omega\text{-mm}$ , which is reasonable for implanted S/D on GaAs and can be further reduced by optimizing the processes of ion implantation and activation during S/D contact fabrication. Contact resistance ( $R_C$ ) of  $0.27 \Omega\text{-mm}$  is extracted from transmission line method. Two third of  $R_{SD}$  is from the access resistance between Ohmic contacts to the channel underneath the gate.  $\Delta L$ , defined as the difference between the mask gate length  $L_g$  and  $L_{eff}$ , is estimated to be  $\sim 0.36 \mu\text{m}$ , due to the lateral dopant diffusion caused by high-temperature activation and/or the lithographic misalignment.

In conclusion, by realizing (111)A nano-facets on (100) surface by anisotropic wet etching and a high-quality epitaxial  $\text{La}_2\text{O}_3/\text{GaAs}$  (111)A interface by ALE, we demonstrate inversion-mode GaAs WaveFETs on GaAs (100) substrates with much larger drain currents than those formed on planar GaAs (100) surface using the same dielectric process. The work opens up a way to improve the III-V device performance by nano-engineering semiconductor 3D structures and interfaces with high-k dielectric.

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