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β-Ga_2O_3 Nanomembrane Negative Capacitance Field-Effect Transistors with Steep Subthreshold Slope for Wide Band Gap Logic Applications

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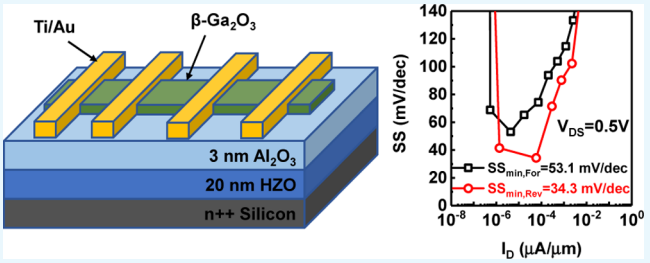
Supporting Information

ABSTRACT: Steep-slope β-Ga_2O_3 nanomembrane negative capacitance field-effect transistors (NC-FETs) are demonstrated with ferroelectric hafnium zirconium oxide in the gate dielectric stack. Subthreshold slope less than 60 mV/dec at room temperature is obtained for both forward and reverse gate-voltage sweeps with a minimum value of 34.3 mV/dec at the reverse gate-voltage sweep and 53.1 mV/dec at the forward gate-voltage sweep at V_{DS} = 0.5 V. Enhancement-mode operation with a threshold voltage of ~0.4 V is achieved by tuning the thickness of the β-Ga_2O_3 membrane. Low hysteresis of less than 0.1 V is obtained. The steep-slope, low hysteresis, and enhancement-mode β-Ga_2O_3 NC-FETs are promising as an nFET candidate for future wide band gap complementary metal-oxide-semiconductor logic applications.



INTRODUCTION

High-temperature solid-state devices and circuits are required for many applications such as in aerospace, automotive, nuclear instrumentations, and geothermal wells.[1,2] Silicon-based complementary metal-oxide-semiconductor (CMOS) technology is not able to operate at such high temperatures, which is limited by its relatively small band gap of 1.12 eV. CMOS circuits using wide band gap semiconductors are promising in these high-temperature logic applications. Monoclinic β-Ga_2O_3 is one of the promising candidates as an n-type channel material because of its ultrawide band gap of 4.6−4.9 eV and high electron mobility of ~100 $cm^2/V{\cdot}s$.[3−10] The ultrawide band gap can suppress the carrier distribution at the tail of Boltzmann distribution at high temperatures. Meanwhile, β-Ga_2O_3 also has the advantage of having low-cost native bulk substrates that can be synthesized in large sizes through melt-grown Czochralski, edge-defined film-fed growth, and floating zone methods.[11−16] To reduce power consumption in wide band gap CMOS logic circuits, enhancement-mode operation with a threshold voltage (V_T) greater than zero and small subthreshold slope (SS) are required, similar to Si CMOS because the enhancement-mode operation and small SS reduce both the static leakage current and the supply voltage.[17] The SS of metal-oxide-semiconductor field-effect transistors (MOSFETs) is limited by the Boltzmann thermal distribution of electrons as $2.3k_BT/q$, which is around 60 mV/dec at room temperature. The SS would increase much more for conventional MOSFETs operated at high temperatures. Negative capacitance FETs (NC-FETs) have been proposed and attracted much attention to overcome the thermionic limit of the SS.[18] In an NC-FET, an insulating ferroelectric material layer is inserted in the gate stack and serves as a negative capacitor so that the channel surface potential can be amplified more than the gate voltage, and hence, the device can operate with the SS less than 60 mV/dec at room temperature. Hafnium zirconium oxide (HZO) is a recently discovered CMOS compatible ferroelectric thin-film insulator with the ability to maintain ferroelectricity with an ultrathin physical thickness down to less than 2 nm.[19−23] Therefore, the integration of wide band gap semiconductors and ferroelectric HZO can reduce the thermionic SS degradation at high temperatures and can reduce power consumption in high-temperature logic applications.

In this paper, we demonstrate β-Ga_2O_3 NC-FETs with ferroelectric HZO in a gate dielectric stack. SS less than 60 mV/dec at room temperature is obtained for both forward and reverse gate-voltage (V_{GS}) sweeps with a minimum value of 34.3 mV/dec at the reverse gate-voltage sweep and 53.1 mV/dec at the forward gate-voltage sweep at V_{DS} = 0.5 V. The enhancement-mode operation is achieved by tuning the thickness of β-Ga_2O_3 with a V_T of 0.47 V for the forward gate-voltage sweep, a V_T of 0.38 V for the reverse gate-voltage sweep, and a low hysteresis less than 0.1 V.

EXPERIMENTS

Figure 1a shows the schematic diagram of β-Ga_2O_3 NC-FETs, which consists of a 86 nm thick β-Ga_2O_3 nanomembrane as the channel, a 3 nm amorphous aluminum oxide (Al_2O_3) layer and

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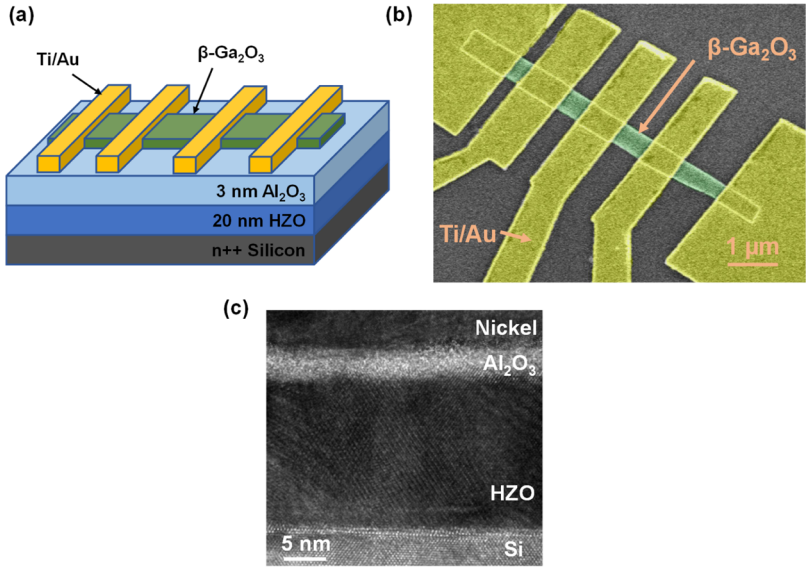

Figure 1. (a) Schematic view of β-Ga_2O_3 NC-FETs. The gate stack includes a heavily n-doped Si as the gate electrode, 20 nm HZO as the ferroelectric insulator, 3 nm Al_2O_3 as the capping layer. Ti/Au (30/60 nm) is used as the source/drain electrodes. Sn-doped n-type β-Ga_2O_3 (86 nm) is used as the channel. (b) Top-view false-color SEM image of representative β-Ga_2O_3 NC-FETs on the same membrane with different channel lengths. (c) Cross-sectional view of the HZO/Al_2O_3 gate stack, capturing the polycrystalline HZO and the amorphous Al_2O_3.

a 20 nm polycrystalline HZO layer as the gate dielectric, a heavily n-doped (n++) silicon substrate as the gate electrode, and a Ti/Au source/drain as the metal contacts. The silicon substrate was first cleaned by an RCA standard cleaning and diluted by an HF dip, to remove organic, metallic contaminants, particles, and unintentional oxides, followed by rinsing in deionized water and drying. The substrate was then transferred to an atomic layer deposition (ALD) chamber to deposit a 20 nm $Hf_{1-x}Zr_xO_2$ film at 250 °C, using $[(CH_3)_2N]_4Hf$ (TDMAHf), $[(CH_3)_2N]_4Zr$ (TDMAZr), and H_2O as the Hf precursor, Zr precursor, and oxygen precursor, respectively. The $Hf_{1-x}Zr_xO_2$ film with x = 0.5 was achieved by controlling the HfO_2/ZrO_2 cycle ratio to be 1:1. To encapsulate the $Hf_{1-x}Zr_xO_2$ film, 3 nm Al_2O_3 was subsequently in situ-deposited by using $Al(CH_3)_3$ (TMA) and H_2O as precursors at the same 250 °C, to prevent the degradation of HZO by the reaction with moisture in air. The amorphous Al_2O_3 layer is also used for capacitance matching and gate leakage current reduction. The importance of this interfacial Al_2O_3 layer on capacitance matching is discussed in detail in ref 23. Rapid thermal annealing in nitrogen ambient was then performed for 1 min at 500 °C to enhance the ferroelectricity.[23] A thin β-Ga_2O_3 nanomembrane was mechanically exfoliated and transferred to the Al_2O_3/HZO/n++ Si substrate from a (−201) β-Ga_2O_3 bulk substrate with an Sn-doping concentration of 2.7×10^{18} cm^{-3} (determined by the $C-V$ measurement[7]). Source and drain regions were defined by electron-beam lithography using ZEP520A as the e-beam resist. An Ar plasma bombardment for 30 s was then applied to generate oxygen vacancies to enhance the surface n-type doping for the reduction of the contact resistance, followed by Ti/Au (30/60 nm) electron-beam evaporation and lift-off processes. Figure 1b shows the false-color scanning electron microscopy (SEM) image of the fabricated β-Ga_2O_3 NC-FETs with four different channel lengths on the same membrane, capturing the β-Ga_2O_3 membrane and the Ti/Au electrodes. Figure 1c shows the cross-sectional transmission electron microscopy image of the HZO/Al_2O_3 gate stack. All device electrical characterizations were carried out at room temperature with a Keysight B1500 Semiconductor Parameter Analyzer and a Cascade Summit probe station.

RESULTS AND DISCUSSION

Figure 2a shows the polarization versus voltage hysteresis loop ($P-V$) for the TiN/20 nm HZO/TiN capacitor at different annealing temperatures. The $P-V$ shows a clear dielectric to ferroelectric transition of HZO after annealing, whereas the $P-V$ shows a weak dependence on the annealing temperature above 400 °C. The metal−insulator−metal capacitors are used for the extraction of Landau coefficients (α, β, and γ) for the ferroelectric HZO layer only. Figure 2b shows the polarization versus voltage ($P-V$) characteristics for the n++ Si/20 nm HZO/3 nm Al_2O_3/Ni stack (the same gate stack of β-Ga_2O_3 NC-FETs) annealed at 450 °C at different voltage sweep ranges. The $P-V$ shows a clear ferroelectric hysteresis loop. The $P-V$ characteristics of a thin-film ferroelectric insulator can be modeled using the Landau−Khalatnikov (L−K) equation.[18] The L−K equation for $P-V$ can be expressed as $V_f = 2\alpha t_f P + 4\beta t_f P^3 + 6\gamma t_f P^5 + \rho t_f \frac{dP}{dt}$, where V_f is the voltage across the ferroelectric insulator, P is the polarization charge, t_f is the thickness of the ferroelectric insulator, $\alpha/\beta/\gamma$ are the Landau coefficients, and ρ is an equivalent damping constant of the ferroelectric insulator. Landau coefficients are extracted directly from the $P-V$ characteristics in Figure 2a on ferroelectric HZO after annealing.[23] In addition, the Landau coefficients are also extracted by fitting to the experimental data using the L−K equation (assuming dP/dt = 0 for static $P-V$ measurement) to be $\alpha = -7.91 \times 10^8$ m/F, $\beta = 1.72 \times 10^{10}$ m^5/F/C,[2] and $\gamma = 0$ m^9/F/C,[4] as shown in Figure 2c. Note that the $P-V$ calculated from the L−K equation shows S-shape, where the negative dP/dV is the negative capacitance, as shown in Figure 2c. However, this negative dP/dV cannot be observed from the experimental $P-V$ (Figure 2a,b) because the negative capacitance state is unstable, which leads to hysteresis in the real experimental $P-V$ measurement. Energy (U) versus charge

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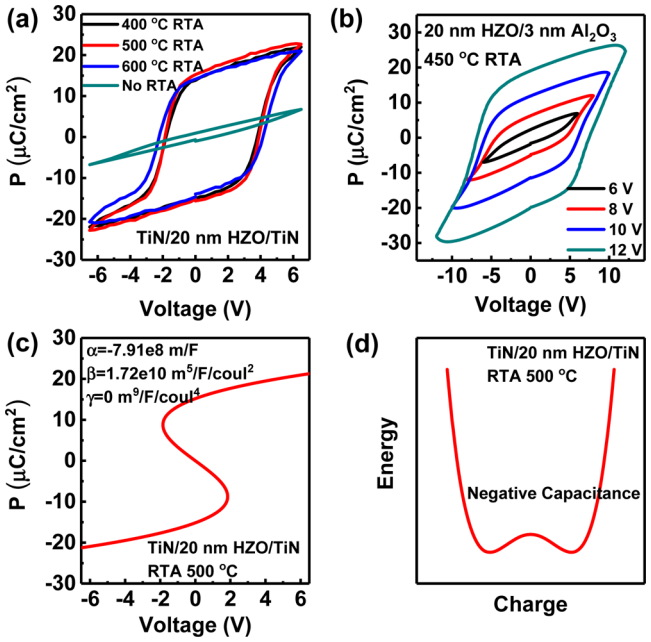

Figure 2. (a) Polarization vs voltage characteristics for the TiN/20 nm HZO/TiN capacitor at different annealing temperatures. The $P-V$ shows a clear dielectric to ferroelectric transition after annealing. (b) Polarization vs voltage characteristics for the 20 nm HZO/3 nm Al_2O_3 stack annealed at 450 °C at different voltage sweep ranges. (c) Landau coefficients extracted from (a) and the corresponding $P-V$. (d) Energy vs charge based on experimental Landau coefficients in Figure 3c. The negative second-order derivative (d^2U/dQ^2) indicates the existence of negative capacitance.

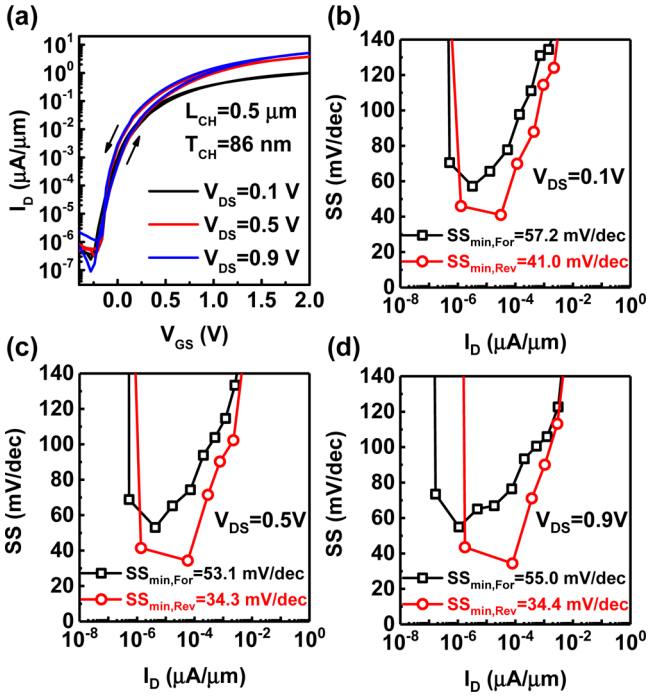

Figure 3. (a) I_D-V_{GS} characteristics in the log scale of a β-Ga_2O_3 NC-FET. This device has a channel length of 0.5 μm and a channel thickness of 86 nm. SS vs I_D characteristics of the same device in (a) at (b) V_{DS} = 0.1, (c) V_{DS} = 0.5, and (d) V_{DS} = 0.9 V. SS less than 60 mV/dec at room temperature is demonstrated for both forward and reverse gate-voltage sweeps.

(Q) is plotted based on the experimental Landau coefficients and calculated using L−K equations as in Figure 2d. The negative second-order derivative (d^2U/dQ^2) also indicates the existence of negative capacitance. The energy of the ferroelectric capacitor tends to stay at the local minimums of the $U-Q$ such that the negative capacitance (where $d^2U/dQ^2 < 0$) becomes unstable. As a result, NC-FETs may exhibit a large hysteresis if the unstable negative capacitance effect is too strong. The key design for the β-Ga_2O_3 NC-FETs in this work is to stabilize the unstable negative capacitance by matching the capacitance of the Al_2O_3 layer (C_{ox}) and the depletion capacitance (C_D) of the β-Ga_2O_3 layer with the capacitance of the ferroelectric HZO layer (C_{FE}). Therefore, low hysteresis and sub-60 mV/dec SS at room temperature can be achieved at the same time.

Figure 3a shows the normalized I_D-V_{GS} characteristics in the log scale of a β-Ga_2O_3 NC-FET. The back-gate bias is swept from −0.4 to 2 V in 40 mV per step, whereas the drain voltage (V_{DS}) is biased at 0.1, 0.5, and 0.9 V. The whole sweep takes roughly 1 min. This device has a channel length (L_{ch}) of 0.5 μm and a channel thickness (T_{ch}) of 86 nm, measured by an atomic force microscope. This particular thickness is chosen to tune the V_T slightly above zero. When the channel is too thick, V_T remains negative such that the device becomes depletion-mode, whereas when the channel is too thin, the conducting current becomes very small.[10] The typical range of the physical width of these nanomembrane devices is 0.3−1 μm, determined by the scanning electron microscope for the normalization of the drain current. The I_D-V_{GS} characteristics were measured in bidirection both forwardly (V_{GS} from low to high) and reversely (V_{GS} from high to low). SS is extracted as a function of I_D for both forward sweep ($SS_{min,For}$) and reverse sweep ($SS_{min,Rev}$) at various V_{DS}. Figure 3b−d shows the SS−I_D characteristics extracted from Figure 3a at V_{DS} = 0.1, 0.5, and 0.9 V, respectively. The device exhibits $SS_{min,For}$ = 57.2 mV/dec and $SS_{min,Rev}$ = 41.0 mV/dec at V_{DS} = 0.1 V, $SS_{min,For}$ = 53.1 mV/dec and $SS_{min,Rev}$ = 34.3 mV/dec at V_{DS} = 0.5 V, and $SS_{min,For}$ = 55.0 mV/dec and $SS_{min,Rev}$ = 34.4 mV/dec at V_{DS} = 0.9 V. SS less than 60 mV/dec at room temperature is demonstrated for both forward and reverse gate-voltage sweeps even at relatively high V_{DS}. Ga_2O_3 MOSFETs with 15 nm Al_2O_3 as a gate dielectric exhibit a minimum SS = 118.8 mV/dec, as shown in Supporting Information section 1. SS−I_D characteristics at different V_{DS} are similar, slightly better at high V_{DS} because of the larger impact of a Schottky barrier at lower V_{DS}. Because of the large band gap of β-Ga_2O_3, the band-to-band tunneling current at high V_{DS} is suppressed.

Figure 4a shows the I_D-V_{GS} characteristics in the linear scale of the same β-Ga_2O_3 NC-FET as in Figure 3. V_T is extracted by linear extrapolation at V_{DS} = 0.1 V for both forward and reverse gate-voltage sweeps. V_T in the forward gate-voltage sweep ($V_{T,For}$) is extracted as 0.47 V, whereas V_T in the reverse gate-voltage sweep ($V_{T,Rev}$) is extracted as 0.38 V. Hence, the enhancement-mode operation with V_T greater than zero for both forward and reverse gate-voltage sweeps is demonstrated. A negligible hysteresis is obtained for both on-state (high V_{GS}, as shown in Figure 4a) and off-state (low V_{GS}, as shown in Figure 3a), except that when V_{GS} is near the threshold voltage region. At the threshold voltage, low hysteresis is achieved to be 90 mV, calculated by using $|V_{T,Rev} - V_{T,For}|$. Note that this hysteresis is negative if we do not take the absolute value because of the gate-voltage-induced polarization charge inside the ferroelectric HZO. This is in stark contrast to the

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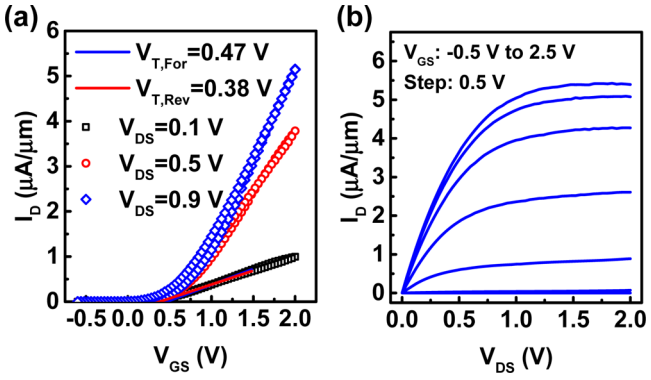

Figure 4. (a) I_D−V_{GS} characteristics in the linear scale of the same β-Ga_2O_3 NC-FET as in Figure 3. V_T is extracted by linear extrapolation at V_{DS} = 0.1 V for both forward and reverse sweeps. (a) I_D−V_{DS} characteristics of the same β-Ga_2O_3 NC-FET as in Figure 3.

conventional hysteresis from MOSFETs with interface and oxide traps, where hysteresis is usually positive because of charge trapping in the defect states. The hysteresis of NC-FETs generally comes from two origins. The first origin is from the unstable negative capacitance state in the ferroelectric insulator ($d^2U_{FE}/dQ^2 < 0$). This hysteresis can be completely removed by well-matched capacitances (C_{FE}, C_{ox}, and C_D) so that $d^2(U_{FE} + U_{ox} + U_D)/dQ^2$ is greater than zero for all Qs for total capacitance to remove the unstable negative capacitance state. The stability condition (static nonhysteretic condition) for 20 nm HZO/3 nm Al_2O_3 has been confirmed to be fulfilled in ref 23 so that it is not the origin of the hysteresis in the β-Ga_2O_3 NC-FETs in this work. The second origin of the hysteresis is a dynamic effect of the measurement because of the ferroelectric dumping factor (ρ) in dynamic L−K equations,[24] which can explain the hysteresis measured in the β-Ga_2O_3 NC-FETs in this work. Figure 4b shows the I_D−V_{DS} characteristics of the same β-Ga_2O_3 NC-FET with V_{GS} from −0.5 to 2.5 V in 0.5 V step and V_{DS} swept from 0 to 2 V. A linear current−voltage relationship at low V_{DS} shows a relatively good contact property at the metal/β-Ga_2O_3 interface. The relative low drain current in this work, compared to that in ref 10, is not clear. The interface situation of β-Ga_2O_3 on the HZO gate stack seems very different from that on SiO_2 in ref 10. The requirement of a thick β-Ga_2O_3 membrane (60−80 nm) to observe the β-Ga_2O_3 enhancement-mode operation indicates the existence of significant interface traps and surface depletion. Although the exact mechanism why interface traps do *not* affect steep-slope observation on β-Ga_2O_3 NC-FETs is not clear at this moment, we suspect that it is related to the ultrawide band gap of β-Ga_2O_3.

CONCLUSIONS

Steep-slope β-Ga_2O_3 NC-FETs are demonstrated with ferroelectric HZO in the gate dielectric stack. SS less than 60 mV/dec at room temperature is obtained for both forward and reverse gate-voltage sweeps with a minimum value of 34.3 mV/dec at the reverse gate-voltage sweep and 53.1 mV/dec at the forward gate-voltage sweep at V_{DS} = 0.5 V. The enhancement-mode operation with a threshold voltage of ∼0.4 V is achieved by tuning the thickness of the β-Ga_2O_3 membrane. In addition, a low hysteresis less than 0.1 V is obtained. The steep-slope, low hysteresis, and enhancement-mode β-Ga_2O_3 NC-FETs are a promising nFET candidate for future wide band gap CMOS logic applications.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsomega.7b01289.

Additional details of Ga_2O_3 MOSFETs with Al_2O_3 only as gate dielectric (PDF)

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Author Contributions

P.D.Y. conceived the idea and supervised the experiments. M.S. studied the ALD of HZO and Al_2O_3. H.Z. exfoliated the β-Ga_2O_3 membrane. M.S. and L.Y. performed the P−V measurement. M.S. performed the device fabrication and electrical characterization and analyzed the experimental data. M.S. and P.D.Y. co-wrote the manuscript, and all authors commented on it.

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Notes

The authors declare no competing financial interest.

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