Supporting Information for:

Indium-Tin-Oxide Transistors with One Nanometer Thick Channel and Ferroelectric Gating

Mengwei Si[1], Joseph Andler[2], Xiao Lyu[1], Chang Niu[1], Suman Datta[3], Rakesh Agrawal[4], Peide D. Ye[1,*]

[1]*School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907, United States*

[2]*School of Materials Engineering, Purdue University, West Lafayette, IN 47907, United States*

[3]*Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556, United States*

[4]*Davidson School of Chemical Engineering, Purdue University, West Lafayette, IN 47907, United States*

* Address correspondence to: yep@purdue.edu (P.D.Y.)

1. Wet Etching of ITO Thin Film

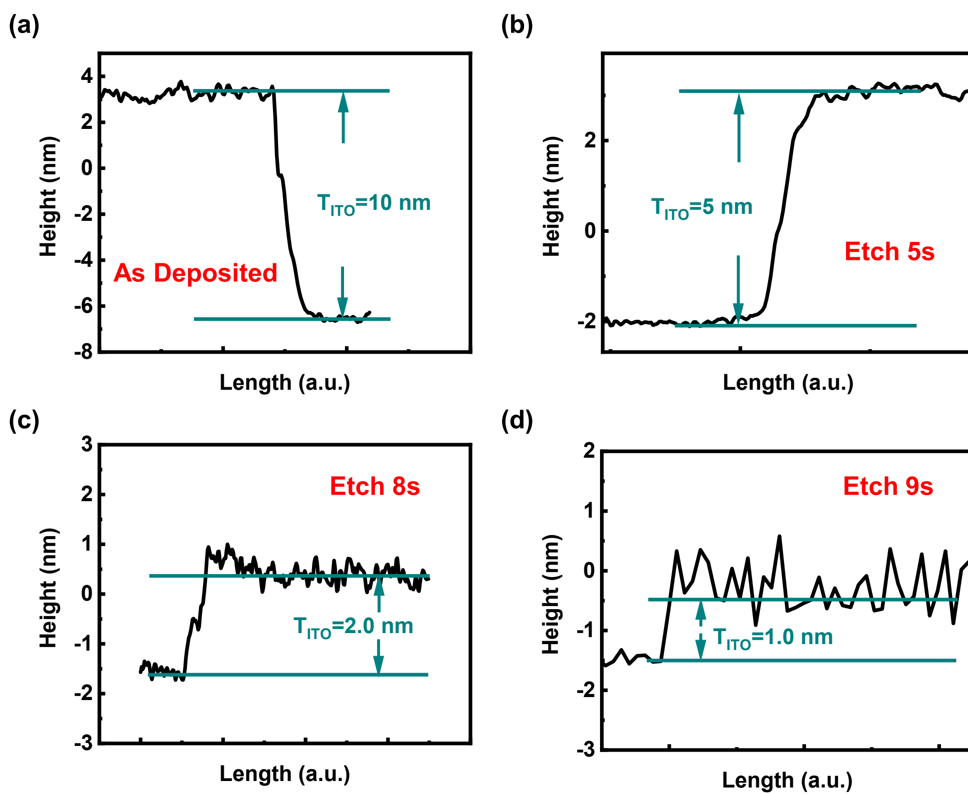

Figure S1 AFM measurement on ITO films with different wet etching times: (a) as deposited, (b) 5s, (c) 8s, (d) 9s, by diluted HCl solution (3.4%).

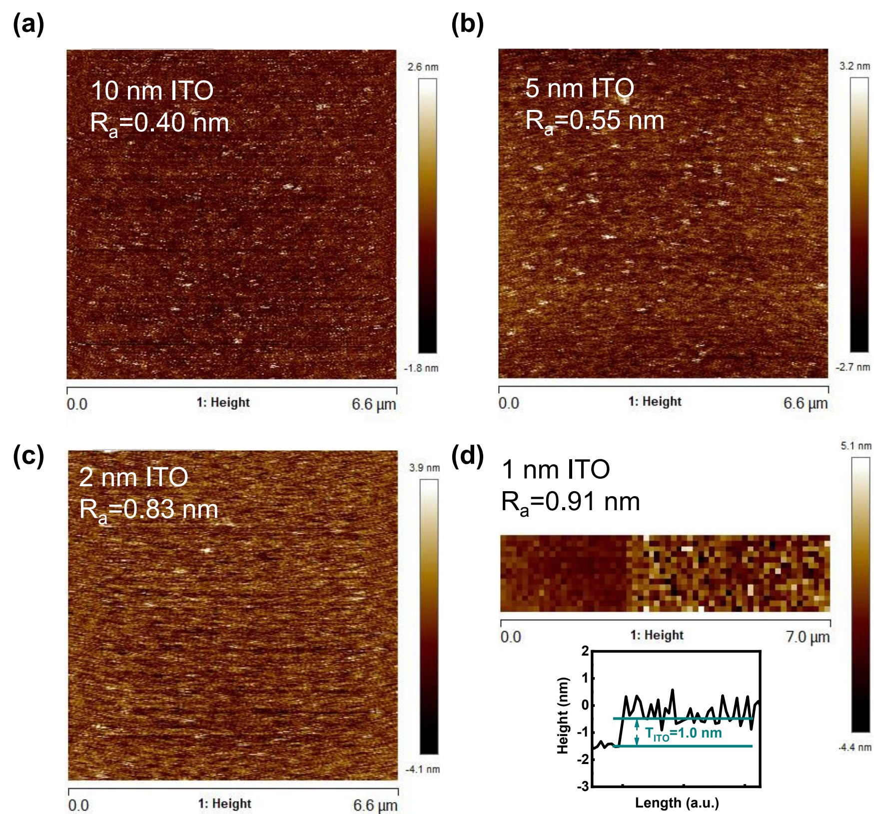

Figure S2 Surface roughness by AFM measurement on ITO films with different thicknesses: (a) 10 nm as deposited, (b) 5 nm, (c) 2 nm, (d) 1 nm.

2. C-V Measurement of the Gate Stack

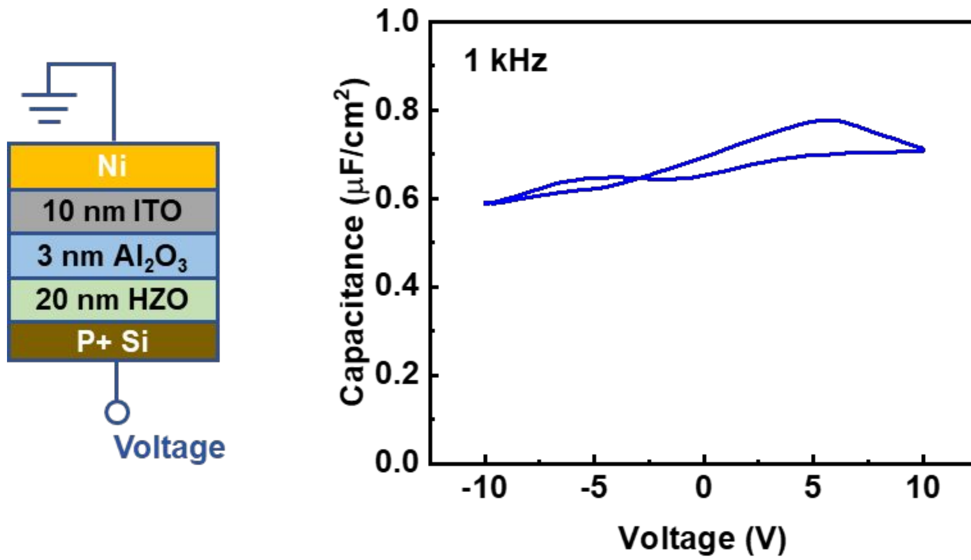

Figure S3 C-V characteristics of p+ Si/20 nm HZO/3 nm Al_2O_3/10 nm ITO stack.

3. I-V Characteristics of ITO Transistors without Channel Recess

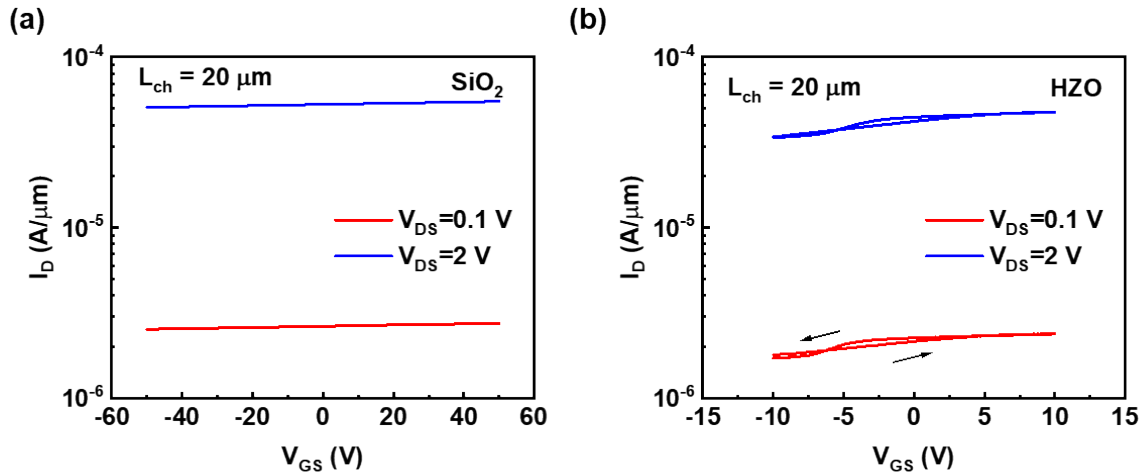

Figure S4 I_D-V_{GS} characteristics of ITO transistors with channel length of 20 μm and channel thickness of 10 nm. (a) 90 nm SiO_2 and (b) 20 nm HZO/3 nm Al_2O_3 are used as gate insulators, respectively.

4. I-V Characteristics of ITO Transistors with Dielectric Gate Insulator

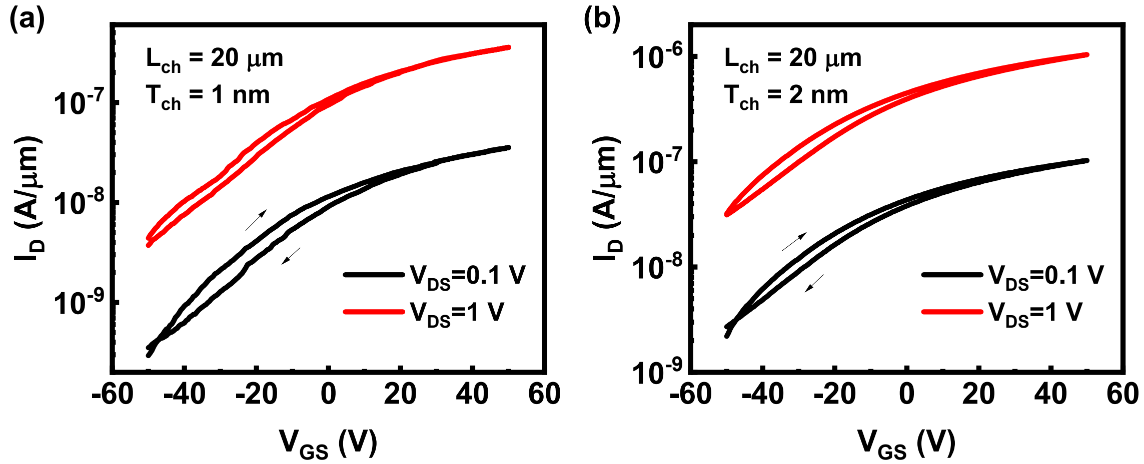

Figure S5 I_D-V_{GS} characteristics of ITO transistors with channel length of 20 μm and channel thickness of (a) 1 nm and (b) 2 nm. 90 nm SiO_2 is used as gate insulators.

I_D-V_{GS} characteristics of ITO transistors with dielectric (DE) 90 nm SiO_2 as gate insulator and L_{ch} of 20 μm and T_{ch} of 1 nm and 2 nm are shown in Fig. S5(a) and S5(b). ITO transistors with FE HZO as gate insulator have much higher current density than ITO transistors with DE SiO_2 as gate insulator, indicating the polarization charges in FE HZO enhance the carrier density in ITO channel.

5. Minor Loops in ITO Transistor with Ferroelectric Gating

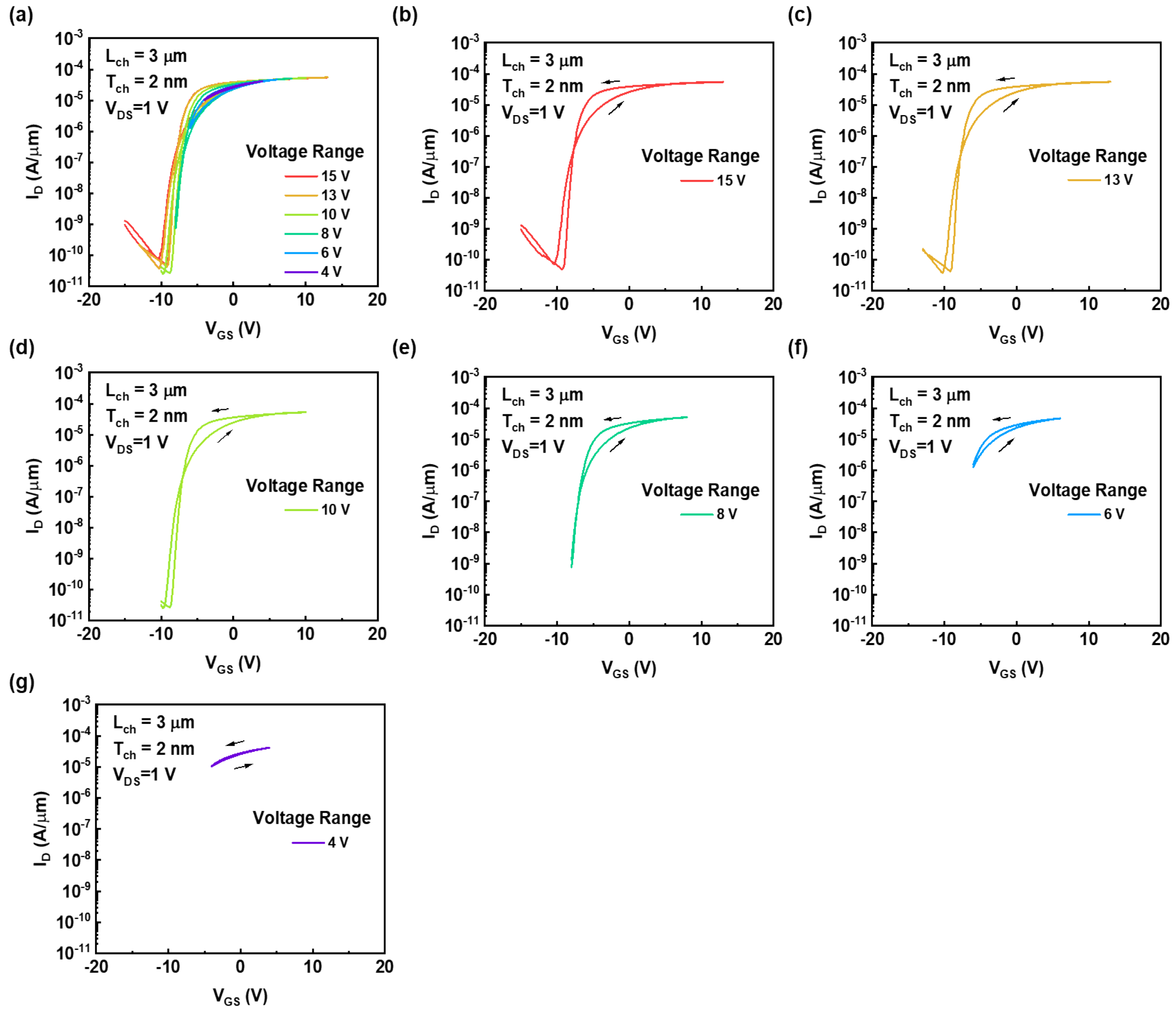

Figure S6 I_D-V_{GS} characteristics of an ITO transistor with channel length of 3 μm and channel thickness of 2 nm,

Fig. S6(a) shows the I_D-V_{GS} characteristics of an ITO transistor with L_{ch} of 3 μm and T_{ch} of 2 nm at V_{DS}=1 V and at different voltage sweep ranges (from 15 V down to 4 V). Fig. S6(b)-(g) are the individual double sweep I_D-V_{GS} curves at different voltage sweep range. As we can see, the counterclockwise hysteresis loop becomes smaller at reduced voltage sweep range, indicating less polarizaiton charge. The device doesn't exhibit memory window as large as ferroelectric field-effect transistors made of Si or Ge,[1,2] suggesting ferroelectric polarization

switching with a wideband gap semiconductor channel may be fundamentally different.

6. Channel Length Scaling of ITO Transistor

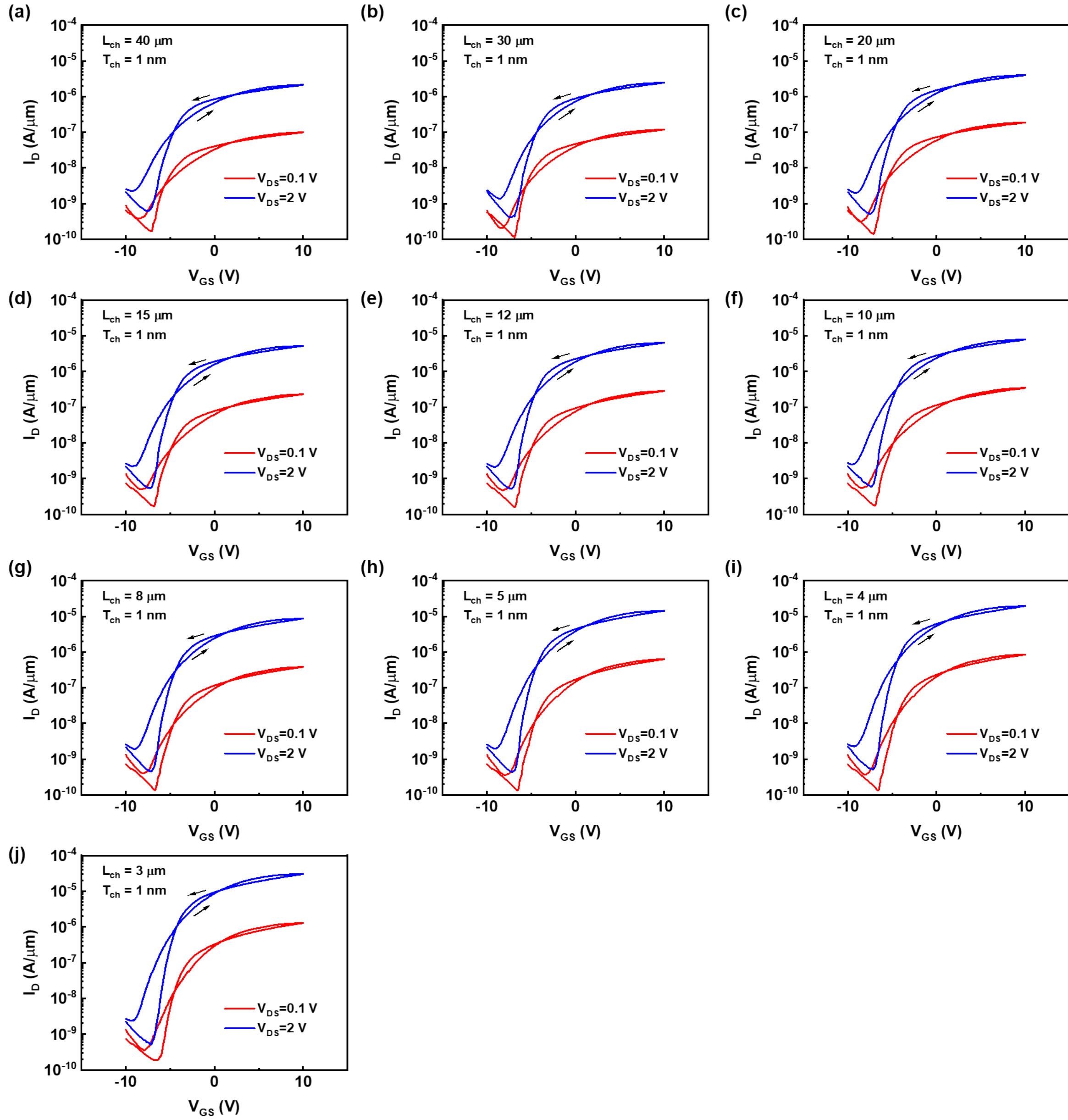

Figure S7 I_D-V_{GS} characteristics of ITO transistors with channel thickness of 1 nm and channel length from 40 μm down to 3 μm.

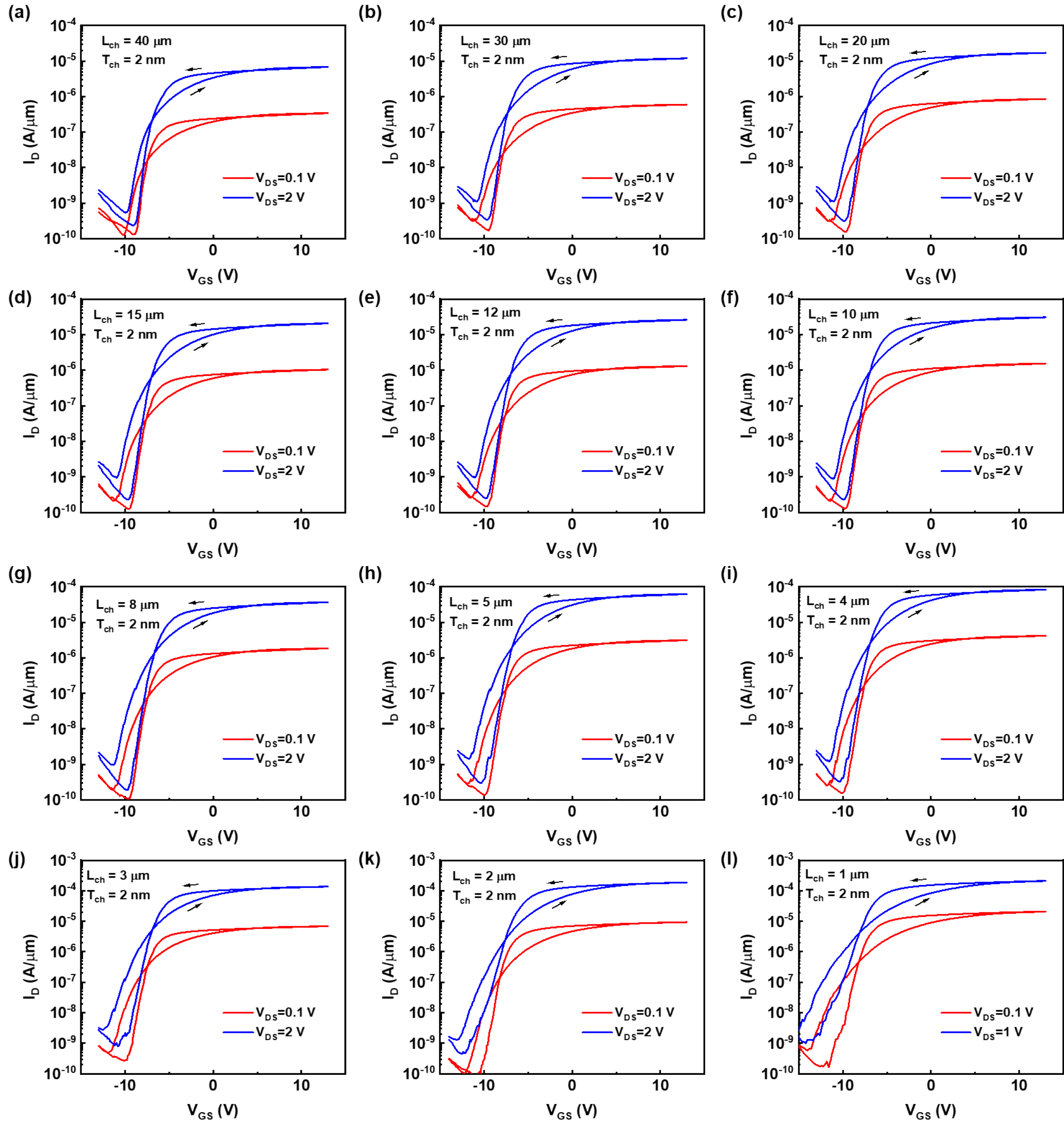

Figure S8 I_D-V_{GS} characteristics of ITO transistors with channel thickness of 2 nm and channel length from 40 μm down to 1 μm.

7. Series Resistance in ITO transistors

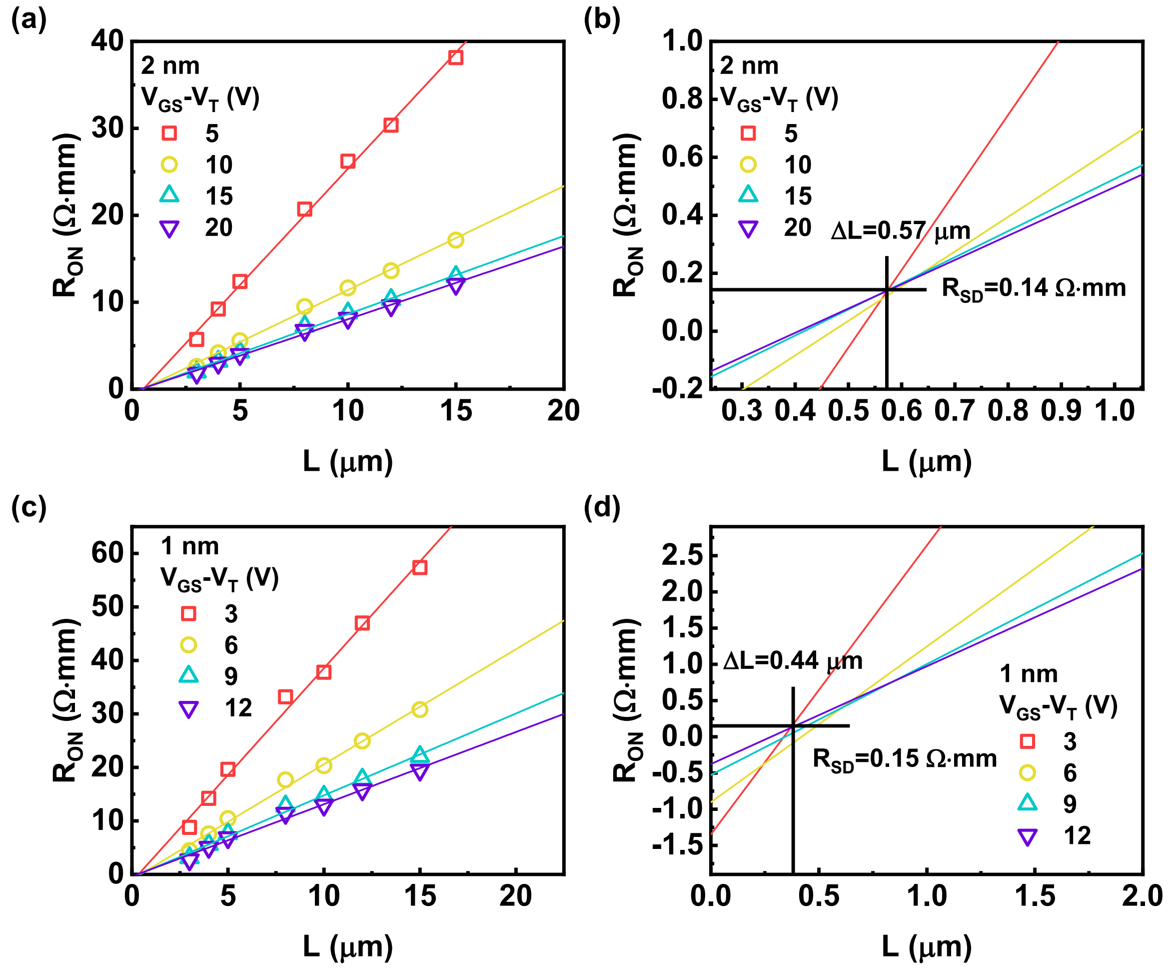

Figure S9 (a) and (c) on-resistance *versus* channel length for ITO transistors with T_{ch} of 2 nm and 1 nm at different V_{GS}-V_T. (b) and (d) Zoomed on-resistance *versus* channel length of (a) and (c). R_{SD} of ITO transistors with 2-nm ITO is extracted to be 0.14 Ω·mm and R_{SD} of ITO transistors with 1-nm ITO is extracted to be 0.15 Ω·mm.

8. Carrier Density of ITO transistors

μ_{eff} of 26.0 $cm^2/V \cdot s$ and 6.1 $cm^2/V \cdot s$ are achieved for 2-nm and 1-nm thick ITO, as shown in Fig. 4. Carrier density can be estimated according to $I_D=n_{2D}q\mu E$, where n_{2D} is the 2D carrier density, q is the elementary charge, μ is the mobility, E is the source to drain electric field. According to this equation, the carrier density in 1-nm and 2-nm ITO channel can be calculated as shown in Fig. S10. Carrier density of 1-nm and 2-nm ITO are similar, with maximum n_{2D} about 0.8×10^{14} $/cm^2$. Therefore, the current density difference between 1-nm and 2-nm ITO comes from the mobility difference. The reduction of drain current density in devices with 1-nm ITO channel is the result of mobility degradation from surface scattering. For 2-nm ITO transistor with 90 nm SiO_2 as gate insulator (Fig. S5(b)), according to μ_{eff}=26.0 $cm^2/V\cdot s$, a maximum n_{2D} of 4.9×10^{12} $/cm^2$ is obtained. For 1-nm ITO transistor with 90 nm SiO_2 as gate insulator (Fig. S5(a)), according to μ_{eff}=6.1 $cm^2/V\cdot s$, a maximum n_{2D} of 7.2×10^{12} $/cm^2$ is obtained. n_{2D} is more than one order of magnitude higher in ITO transistor with FE gating ($n_{2D} > 8\times10^{13}$ $/cm^2$). Such difference cannot be the result of different EOT. For example, for 50 V on 90 nm SiO_2, the voltage/EOT is about 0.6 V/nm; for 13 V on 20 nm HZO/3 nm Al_2O_3, the voltage/EOT is about 2.4 V/nm. The difference in displacement field is only 4 times. Therefore, only EOT difference itself cannot lead to the enhancement demonstrated in this work. Considering the low current density in ITO transistors with SiO_2 as gate insulator, as shown in Fig. S5(a) and S5(b), the high carrier density in ITO transistor with FE HZO as gate insulator comes from the enhancement by FE polarization.

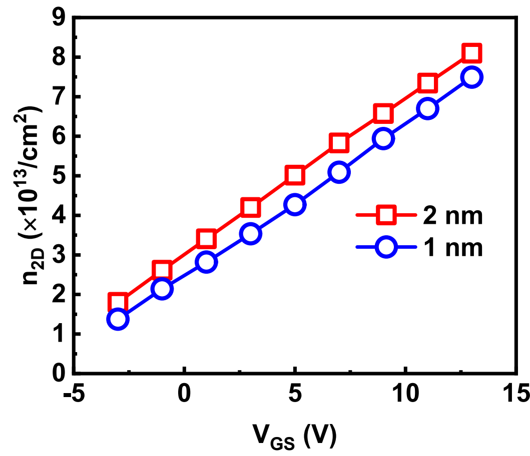

Figure S10 Carrier density *versus* gate voltage for 1-nm and 2-nm ITO.

9. Device Variations

The ITO deposition was done by sputtering so that this technology can be used for large-area fabrication process. Fig. S11 shows I_D-V_{GS} characteristics of 13 ITO transistors with channel thickness of 2 nm and channel length of 3 μm, showing similar switching characteristics. The device-to-device variation comes from variation in wet etching process. Such variation can be further improved by introducing dry etching or re-growth source/drain process.

The off-state current in this work comes from the gate leakage current through FE HZO, as shown in Fig. S12. I_G and I_D at off-state are very similar. Therefore, the off-state current variation in this work originates from the gate leakage current variation.

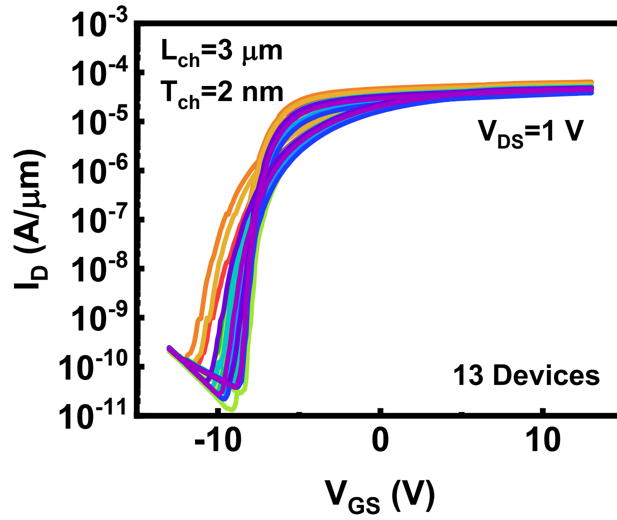

Figure S11 I_D-V_{GS} characteristics of 13 ITO transistors with channel thickness of 2 nm and channel length of 3 μm.

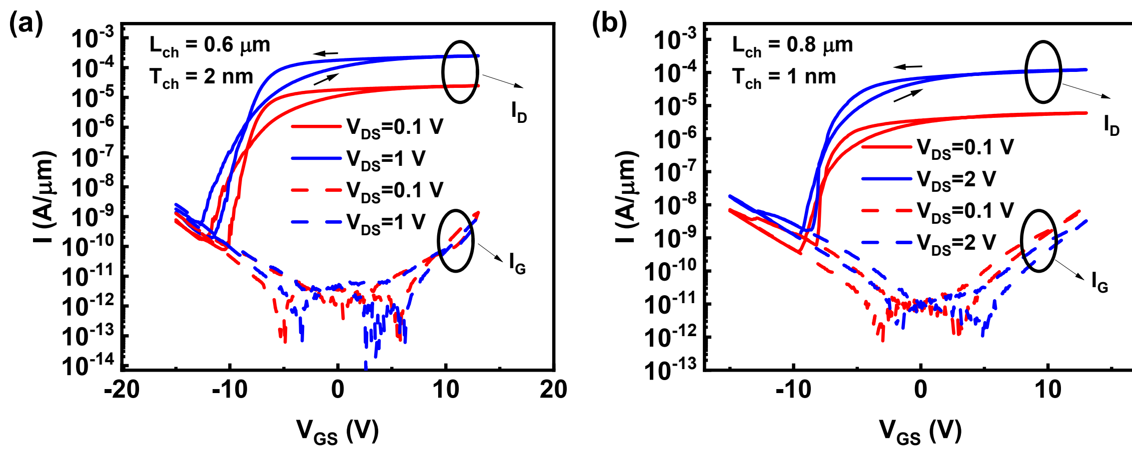

Figure S12 I_D-V_{GS} and I_G-V_{GS} characteristics of (a) an ITO transistor with channel thickness of 2 nm and channel length of 0.6 μm and (b) an ITO transistor with channel thickness of 1 nm and channel length of 0.8 μm.

Reference

(1) Müller, J.; Böscke, T. S.; Schröder, U.; Hoffmann, R.; Mikolajick, T.; Frey, L. Nanosecond Polarization Switching and Long Retention in a Novel MFIS-FET Based on Ferroelectric HfO_2. *IEEE Electron Device Lett.* **2012**, *33*, 185–187.

(2) Chung, W.; Si, M.; Ye, P. D. First Demonstration of Ge Ferroelectric Nanowire FET as Synaptic Device for Online Learning in Neural Network with High Number of Conductance State and G_{Max}/G_{Min}. In *2018 IEEE International Electron Devices Meeting (IEDM)*; IEEE, 2018; pp 15.2.1-15.2.4.